Development of decoration and preferential-etching methods for delineation of crystal defects in semiconductor materials

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By

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D30

Well done is better
than well said.

BENJAMIN FRANKLIN

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Abbreviations

A	preexponential factor (Arrhenius equation)
AFM	atomic force microscopy
Approx.	approximately
BESOI	bonding and etch-back silicon-on-insulator
BMD	bulk micro defects
BOX	buried oxide
BSE	back-scattered electrons
CA	chloranil
CDF	Cu-contamination-induced defects in the SOI-film/BOX interface
CDS	Cu-contamination-induced defects in the BOX/Si substrate interface
Conc.	concentration
COP	crystal originated particle
CP (4)	chemical polishing etchant/etches (4)
Cu	copper
CZ	Czochralski
DD	defect density
dil.	diluted
E_a	activation energy
EDX	energy dispersive X-ray spectroscopy
e.g.	exempli gratia (for example)
ETSOI/UTBOX	extra thin SOI/ultra thin BOX
ΔF	acting force

fcc	face-centered cubic
Fig.	figure
FZ	float-zone
G	axial temperature gradient
GeOI	germanium-on-insulator
HAc	acetic acid
HF	hydrofluoric acid
IARC	International Agency for Research on Cancer
IC	integrated circuit
k	rate coefficient
K	equilibrium constant
K_C	spring constant
Li	lithium
LT	layer thickness
LT_{res}	residual layer thickness
MCZ	magnetic Czochralski
Min	minute
MOSFET	metal-oxide semiconductor field-effect transistor
nm	nanometer
PE	primary electron
ppm	parts per million
o. D.	other defects
o. OiSF	other OiSF
OPE	organic peracid etch
OSF/OiSF	oxidation-induced stacking faults

Ox	oxidizing component
r	removal rate
R	gas-law constant (8.414 $JK^{-1}mol^{-1}$)
Ref	reference
REM	Rasterelektronenmikroskop
RF	radio frequency
RTP	rapid thermal processing
S	selectivity
SE	secondary electron
SEM	scanning electron microscopy
Si	silicon
SIMOX	separation by implanted oxygen
SOI	silicon-on-insulator
sSOI	strained silicon-on-insulator
SF	stacking fault
t	etching duration
T	temperature
T_{etch}	etching time
Tab.	table
TEM	transmission electron microscopy
TD	threading dislocation
V	pulling rate
vs.	versus
µm	micrometer
σ	standard deviation

Contents

1 Introduction

The transition from the development of transistors as semiconductor devices to their integration in electronic circuits took a long time [1]. It was in 1947 that Walter Brattain and John Bardeen took the first steps which finally led to the discovery of the transistor effect. But soon limits in the combination of transistors were reached and the invention of the integrated circuit (IC) opened new ways to increase the number of transistors in a semiconductor [2, 3]. In 1960 the MOSFET (metal-oxide semiconductor field-effect transistor) was invented by Dawon Kahng who put an insulating layer on a semiconductor surface. The MOSFET has three different electrodes: the source (S), the gate (G) and the drain (D), and is generally implemented in microprocessors. The advantage of this was that the transistors became smaller and faster and used less energy.

The next major development may be attributed to Gordon Moore who, in 1965, managed to assemble more elements onto an integrated circuit structure [4]. He predicted that costs would be diminished, accompanied by the increase of circuit functions on one semiconductor substrate. At the same time the costs per component could be reduced as well. Another prediction of him was what is known as “Moore’s Law” and which said that the number of active transistor devices on a single IC would double every year. Moore’s Law was the basic idea over the last forty years and simply meant “the smaller, the faster”. This tendency in progress is supposed to reach its end when the scale comes to atomic dimensions in about 10 to 15 years and this would also mean that “Moore’s Law” would not be valid anymore. However, modern microprocessors contain billions of transistors as the feature size of device structures was reduced to the nanometer level. Despite all hopes and expectations in the progress in semiconductor technology, transistors based on MOS technology are still essential in this field. However, to achieve progress in device performance it was also required to introduce a variety of novel materials and sophisticated device concepts. Among those is the use of HfO_2 or ZrO_2 as an insulator for the gate dielectric of MOSFETs instead of the traditional SiO_2 and the replacement of silicon substrates by Silicon on Insulator (SOI) material. The benefits of SOI among other features are low power consumption and better electrostatic control.

Standard SOI material consists of a mono-crystalline silicon substrate, covered by an insulating layer (SiO_2), called buried oxide (BOX), on which a monocrystalline silicon layer – the SOI film – is mounted by a bonding process. Today most of the SOI wafers are produced by the SOITEC Smart-Cut^{TM} technology.

Silicon produced for the microelectronic industry is seen as the most perfect material manufactured today, however, even this pure material shows defects which come into existence when processed. These defects impair the function and reliability of ICs. It is absolutely necessary to find and characterise the various crystal defects as their density is an indication of the quality of the substrate. The Czochralski (CZ) procedure to obtain pure monocrystalline silicon from a melt is one source of the crystal defects that are found in SOI films. The relation between the pulling rate (V) and the thermal gradient of the growing CZ crystal at its solid liquid interface essentially define the kind, the size, the amount and the distribution of some of the grown-in crystal defects. In addition, process-induced defects are formed during the high-temperature processing steps used for buried-oxide formation, bonding and final planarization of the SOI wafers.

The most common way to detect and characterise the crystal defects is to use an etching solution which can delineate them as pits in SOI and sSOI films. In general etching solutions that have been employed so far have a strong oxidizing agent that converts elemental silicon Si(0) into the oxidation state Si(IV). They also contain hydrofluoric acid which dissolves the product of oxidation and last but not least they contain a diluent such as water or acetic acid. The standard etching solutions for defect delineation in thin films such as SOI and sSOI are various diluted versions of the Secco solution. Most etching solutions (such as Secco) in use contain chromium (VI) which has been found to be extremely toxic and carcinogenic, as well as environmentally dangerous, facts that make it necessary to restrict its use or even to find a suitable substitute.

The new etching solutions of choice should therefore be free of chromium (VI) in their composition to protect both human health and the environment [5]. Moreover lower etching rates will make it possible to better control the etching time. Further qualities should be an improved etch homogeneity and etch sensitivity in order to better define the various crystal defects, and a considerable degree of stability.

However, nanometer-sized crystal defects (below 20 nm) are scarcely revealed by defect etching alone. Copper decoration is a well established method to facilitate the delineation of even small defects in the bulk of silicon wafers. It is well known that copper precipitates as silicide (Cu_3Si) on sites provided by grown-in or process-induced crystal defects resulting in the magnification of the defects and such improved delineation after etching as to make them detectable on inspection by a light optical microscope or a scanning electron microscope (SEM). A shortcoming of copper decoration is its tendency to form artefacts due to copper precipitation at the wafer surface when the copper concentration used is too high. Artefacts are not easily distinguished from delineated defects and the result could be the determination of defect densities that are misleading.

The aim of this thesis is to show that the processes of decorating and etching can be successfully combined for the best possible delineation of crystal defects in SOI and sSOI. Ideally this should involve a well balanced solution that would decorate all existing crystal defects and at the same time contain the most adequate concentration of copper to avoid artefact formation.

Copper decoration experiments were performed on SOI with different SOI film layer thicknesses (60 to 1400 nm) and correspondingly varying BOX layer thicknesses (145 to 1 000 nm), testing both the standard etchant dil. Secco (0.04 M Cr (VI)) and several novel chromium-free etching solutions to achieve improved defect delineation. The BOX layer in SOI can be a slight to strong diffusion barrier depending on its thickness, hence, the decoration conditions were also optimized with regard to the BOX layer. Two different copper decoration procedures were tested and compared whereby the focus was on decoration via furnace annealing.

The chromium-free Organic Peracid Etch (OPE) etching solutions only reveal threading dislocations (TD) but not stacking faults (SF) in sSOI material. In general, stacking faults are decorated with preference, hence, a combination of copper decoration with preferential etching using different OPE solutions was tried out, to delineate both of the above-named defects as an alternative to the dilute Secco (0.04 M Cr (VI)) for defect delineation in sSOI materials.

A further decoration metal, lithium, was tested as well with regard to SOI as an alternative almost artefact-free defect decoration procedure.

Furthermore, parameters such as removal rate, selectivity and activation energy for the etching process were studied with regard to their influence on preferential etching of intentionally metal decorated crystal defects in SOI wafers.

Defect densities were routinely determined using a light optical microscope. Selected defects were inspected more precisely via SEM and atomic force microscopy (AFM) and selected SOI samples were analysed using secondary ion mass spectrometry (SIMS).

2 Wafer fabrication

For silicon wafer manufacture, high purity of monocrystalline silicon (99.999 999 999%) is required. Fig. 2.1 shows a short summary based on a flow diagram for the semiconductor silicon preparation process [6]:

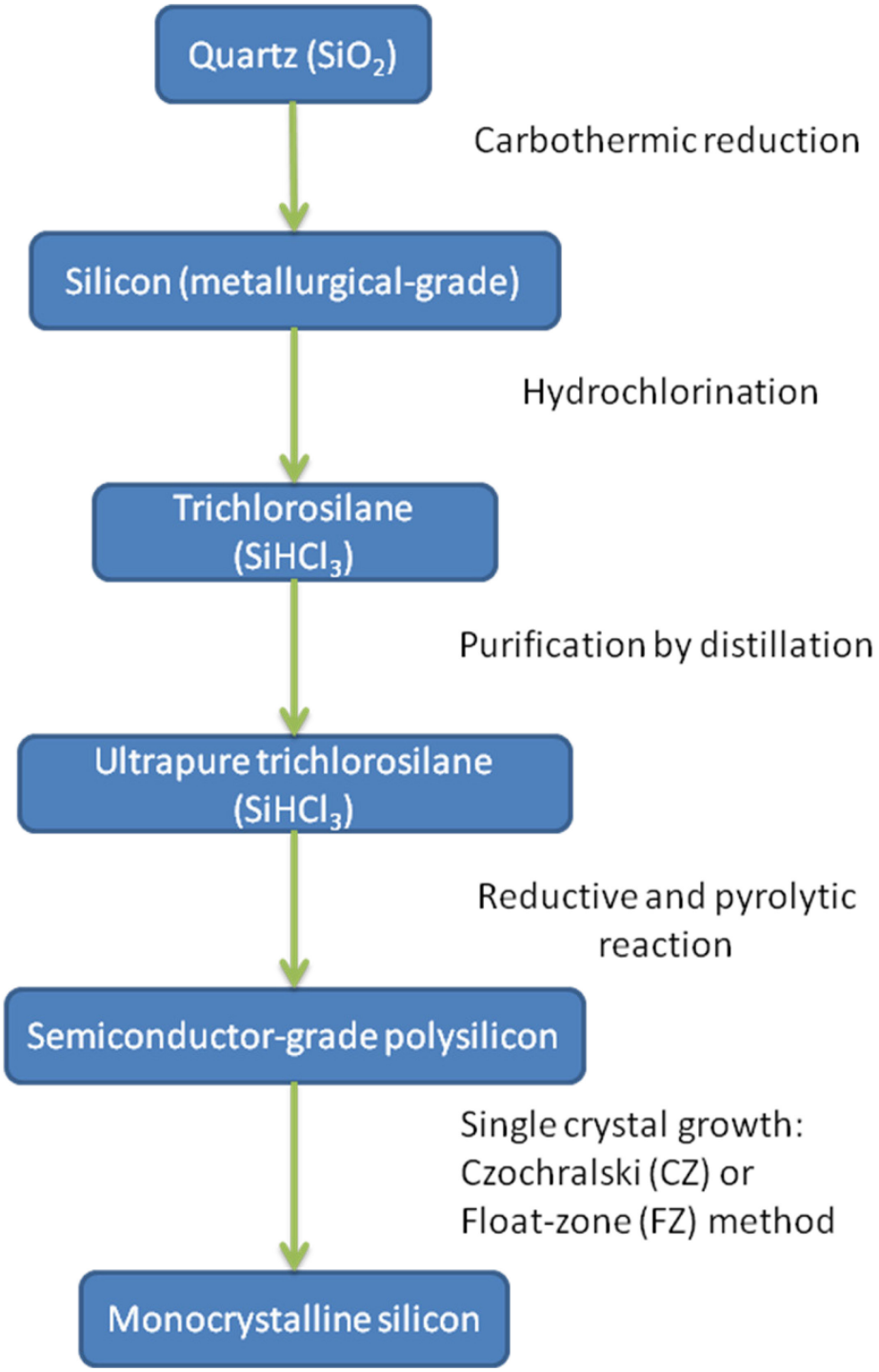


Fig. 2.1 Diagram for the semiconductor silicon preparation process.

2.1 The production of high-purity silicon

The second most abundant element on earth is silicon which is the basic material for the wafer manufacturing process. More than 90% of the earth's crust is comprised of silica or silicate.

Quartz is used as the raw material for the preparation of high-purity silicon. Quartz is reduced by carbon in an arc furnace by reduction reactions which proceed at temperatures ranging from 1 500-2 000 °C [7]:

$$SiO_2 + 2\ C \rightleftharpoons Si + 2\ CO$$

The obtained metallurgical-grade silicon offers a purity of just 90%, containing low parts of metal impurities like iron and aluminum and signs of non-metals like boron or phosphorus. For the production of wafers a purity of 99.999 999 999% is essential to obtain semiconductor-grade silicon wherefore a subsequent treatment of the raw silicon is necessary. Hence, the next step is the chemical reaction between the technical silicon and hydrogen chloride using temperatures of about 300-400 °C:

$$Si + 3\ HCl \rightleftharpoons SiHCl_3 + H_2$$

However, by-products such as monosilane (SiH_4), silicon tetrachloride ($SiCl_4$) and dichlorosilane (SiH_2Cl_2) are also formed. The obtained trichlorosilane ($SiHCl_3$) is subsequently distilled for the purification removing impurities such as chloride compounds of metals like iron and aluminum (as $FeCl_2$, $AlCl_3$). The trichlorosilane (boiling point about 32 °C) is removed by fractional distillation from the reaction mixture to get vaporized and mixed with hydrogen in a deposition reactor. The decomposition of trichlorosilane occurs at thin heated (1 100 °C) silicon rods within the deposition reactor under formation of silicon. These chemical reactions are summarized as follows:

$$4\ SiHCl_3 \rightleftharpoons Si + 3\ SiCl_4 + 2\ H_2$$

$$SiCl_4 + H_2 \rightleftharpoons SiHCl_3 + HCl$$

The ultra-pure silicon (99.999 999 999%) is deposited at the rods and is ready for the next step: the growth of single crystals. Two crystal pulling techniques are used for the preparation of silicon single crystals:

- The Float-Zone (FZ) method and
- The Czochralski (CZ) method

2.2 The Czochralski (CZ) method

The CZ method [8, 9] dominates the production of monocrystalline silicon for wafer manufacturing. About 95% of single crystal silicon is produced through this method which was discovered and developed in 1916 by Jan Czochralski. Teal and Little modified Czochralski´s basic principles and developed the pulling method which was successfully applied for growing single crystals of germanium in 1950. The CZ crystal growth is divided into three steps:

- Melting polysilicon
- Seeding
- Growing

Fig. 2.2. shows a view of a CZ growth system:

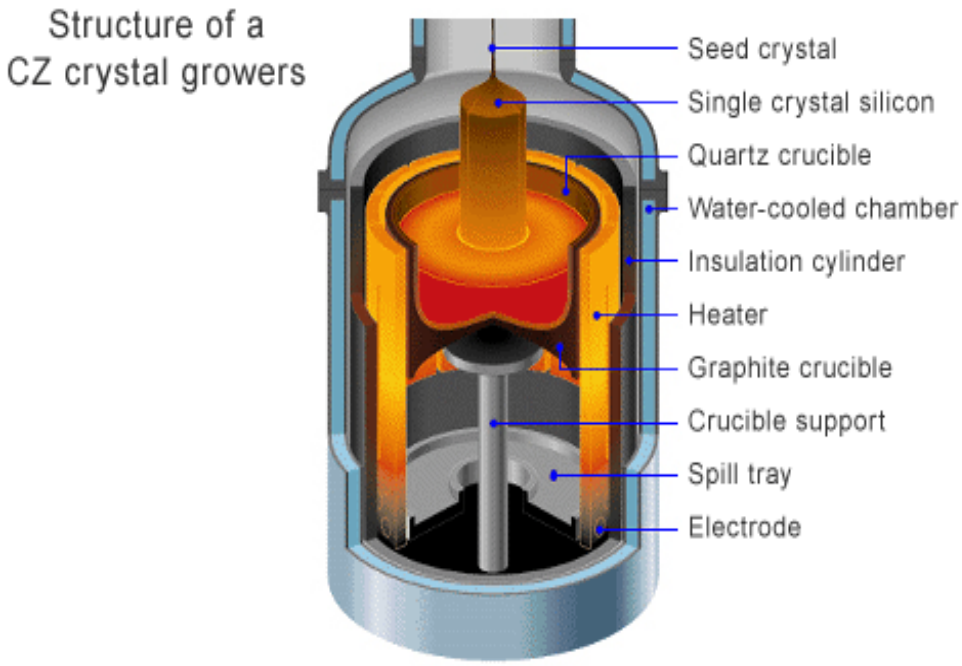


Fig. 2.2 Structure of a CZ crystal grower.[1]

The polycrystalline silicon is placed in a quartz crucible, which is surrounded by a graphite crucible, and heated in an inert gas atmosphere using temperatures above 1 420 °C (melting point of silicon). The high temperatures for the melting process are necessary to provide both complete melting and prevention of formation of tiny bubbles. Further reaction products such as SiO or CO are removed by the inert gas argon. In the next step a thin seed crystal is

[1] from http://www.sumcosi.com/english/products/process/step_01.html

dipped into the melt until it begins to melt itself. This procedure is called seeding. The seed is drawn from the melt to form the neck by gradually reducing the diameter under stable melt conditions (Fig. 2.3). This “necking” process is important to provide dislocation-free crystal growth. After the necking process the crystal diameter is increased gradually to obtain and grow both the conical part and shoulder. The orientation of the rotating seed crystal determines the orientation of the growing crystal. The diameters of the growing crystal are controlled by the pulling rate and melt temperature. Decreasing the pulling rate or the melt temperature an increase of the diameter is achieved.

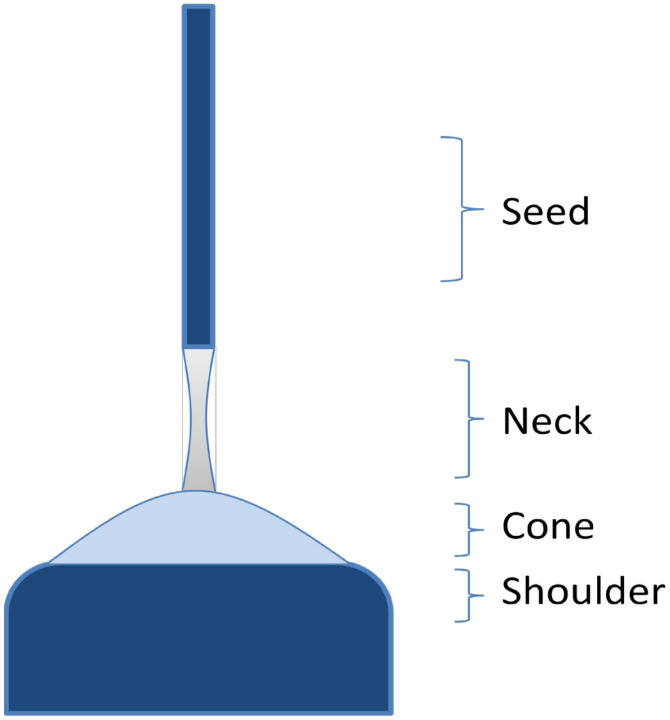


Fig. 2.3 Scheme of a CZ growth silicon crystal.[2]

Further development of this procedure to obtain 300 mm diameter CZ growth was necessary wherefore magnetic fields were added. This reworked procedure is known as the magnetic CZ method (MCZ) offering these advantages:

- Control heat and mass transfer in the large mass volumes
- The transport of oxygen is reduced by convection whereby a lower oxygen concentration is obtained
- Lower defect formation

[2] modified from A. Shimura, Semiconductor Silicon Crystal Technology

The cylindrical part is grown with a constant diameter by controlling the pulling rate and the melt temperature. Before finishing the growth process the crystal diameter must be reduced gradually to form an end-cone to prevent thermal shock and consequently the formation of slip dislocations at the tail end. Subsequently the silicon crystal can be removed from the melt without creation of defects mainly such as dislocations.

2.3 The Float Zone (FZ) Method

The concentration of impurities such as carbon and oxygen (oxygen concentration: in the range of 10^{16} atoms/cm^3) is lower using the FZ method [10] compared to the CZ method (high oxygen concentration of 10^{18} atoms/cm^3) due to the absence of the contact between silicon melt and a contaminating crucible. Hence, FZ silicon is a high purity alternative to the CZ silicon.

A moveable induction coil is used to melt a silicon rod at one end. Then the molten tip is contacted and fused with a single crystal seed with the desired crystal orientation (Fig. 2.4). The induction coil is moved along the rod, melting the zone it surrounds. The molten zone solidifies as the induction coil moves away and grows as an extension of the seed crystal. The silicon rod rotates in a protective atmosphere and the melting zone moves from one end of the rod to the other. After seeding a thin neck of about 2 or 3 mm in diameter is grown (length: 10-20 mm). This leads to the prevention of the formation of dislocations which occur in the newly grown single crystal during the seeding process due to the thermal shock.

The impurities present are less soluble in the crystal than in the melt and are therefore drawn with the melting zone to the end of the rod. This results in a very low concentration of foreign atoms in the silicon crystal lattice. However, for technical reasons the diameter of the single crystal ingot is much smaller than that of the CZ produced ingot leading to higher costs for wafers which are manufactured by the FZ process.

The purity of the FZ material causes a resistivity of more than 200 Ωcm. That is why FZ silicon can be used for

- power devices
- high efficiency solar cells
- radio frequency (RF) wireless systems

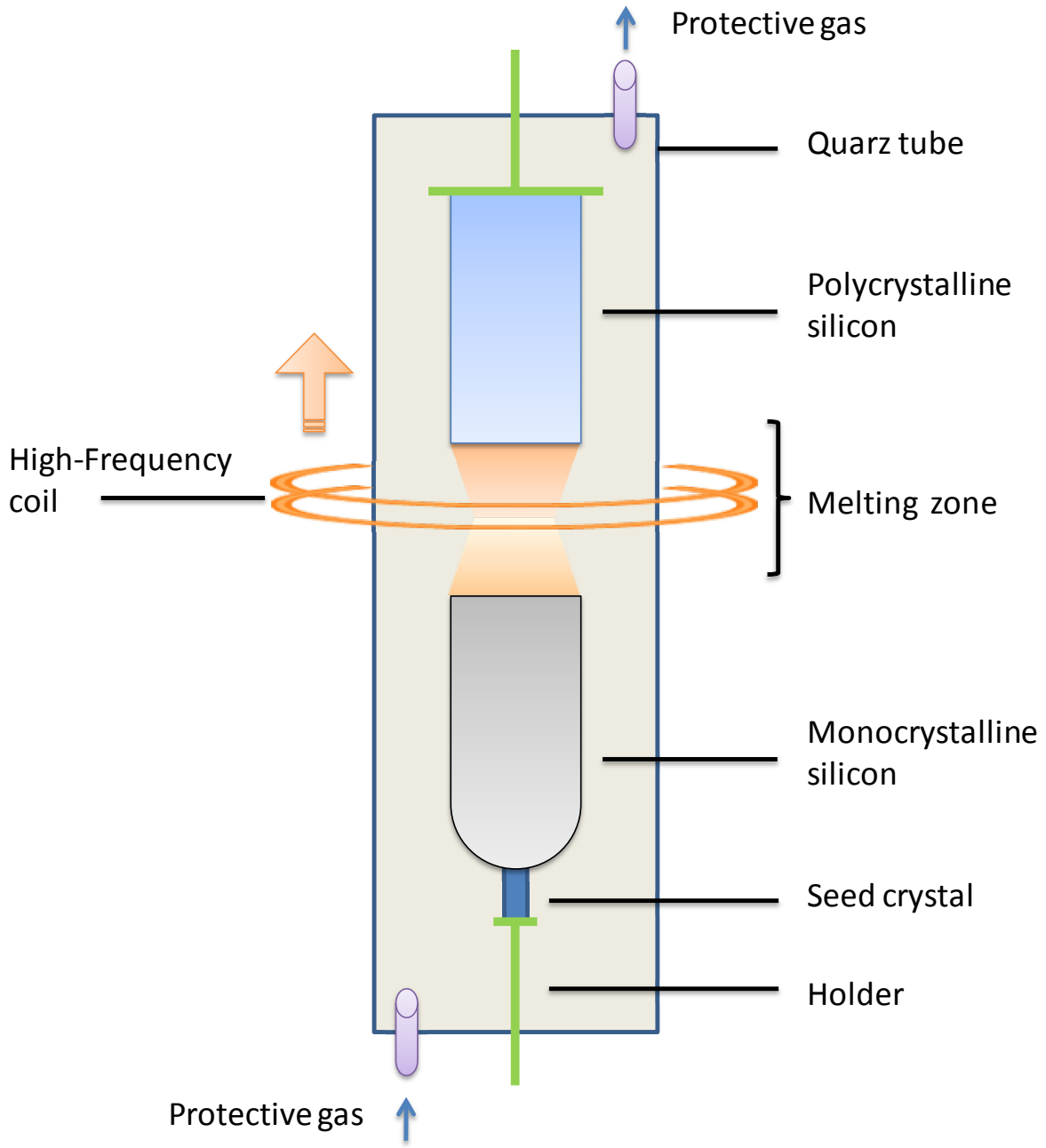


Fig. 2.4 Scheme of the FZ process.[3]

[3] modified from H. Kück izfm, University of Stuttgart

2.4 Manufacturing of novel silicon wafers

The increasing request for more powerful microelectronic devices for improved multimedia functions led to the development of low power, low voltage and high performance circuits in the IC industry.

Novel substrate materials such as Silicon On Insulator (SOI), Strained Silicon On Insulator (sSOI) or Germanium On Insulator (GeOI) are developed to overcome the limitations of conventional silicon substrates or epitaxial wafers regarding further progress in the performance of microelectronic devices.

2.4.1 Silicon On Insulator (SOI)

The SOI wafer is composed of a thin single-crystalline silicon layer on top of an insulator, generally silicon dioxide, referred to buried oxide (BOX) to minimize the capacitance of a transistor [11-13] (Fig. 2.5). A silicon bulk in the lower layer acts as the substrate. Standard silicon wafers offer a total thickness of approximately 750 µm. However, the layer thickness of the required SOI is just in the range of some ten nm.

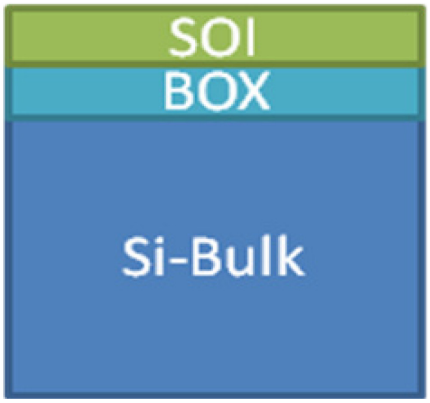


Fig. 2.5 Scheme of a SOI wafer.

The manufacturing of SOI wafers occurs via the following methods:

- SIMOX process
- BESOI process
- Smart-Cut™ process
- Smarter-Cut™ process

2.4.2 SIMOX process

The Separation by Implanted Oxygen (SIMOX) [13-15] process can be classified as follows (Fig. 2.6):

- Implantation of O^+-ions to form the BOX (buried oxide) layer
- Annealing using high temperatures about 1 320 °C

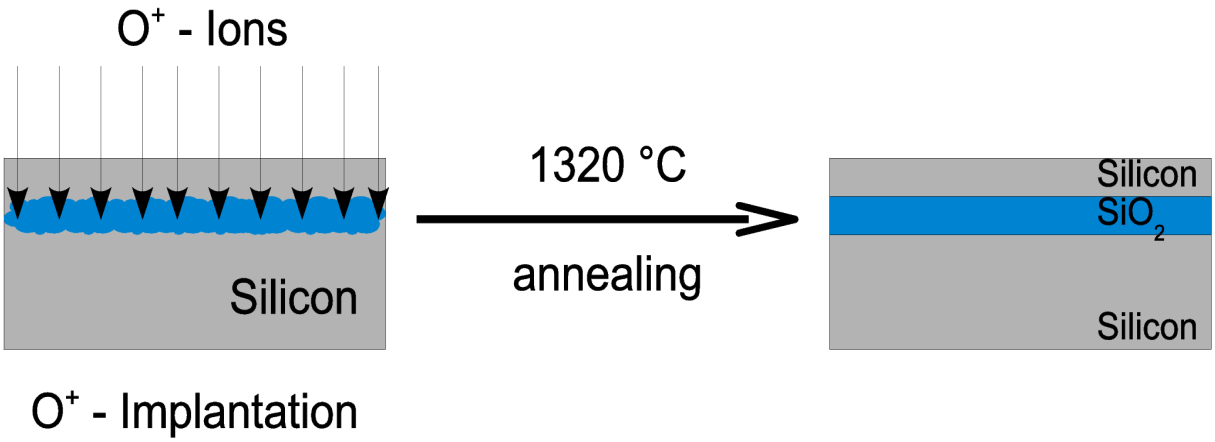


Fig. 2.6 Scheme of the SIMOX process.[4]

The SIMOX process was one of the first methods for SOI wafer manufacturing. This technique has lost its significance due to the development of the Smart-Cut™ process caused by unsuitable high costs for the industrial production of SOI wafers.

The thickness of the required BOX layer is controlled by:

- The oxygen dose used (around 1.4 x 10^{18} O^+ ions/cm^2)
  novel process: lower oxygen implantation dose about 4 x 10^{17} O^+ ions/cm^2, resulting in BOX layer thicknesses in the range of 80–100 nm
- The temperature during the implantation procedure
  a high annealing temperature generates both an even and an stoichiometric BOX layer
- The kinetic energy (around 200 keV) of the ions define the depth of the BOX layer

[4] modified from A. J. Auberton, *Proceedings of the European Solid State Device Research Conference (IEEE)* (1996)

The main drawback of this procedure is its tendency to induce much larger implantation damages compared to the Smart-Cut^{TM} process caused by the significantly larger size of the O^+-ions in contrast to the hydrogen ions.

Further development of this procedure by lowering the oxygen implantation dose leads to a decrease of the defect density and consequently to an increase of the silicon crystal quality.

A high annealing temperature (1 320 °C) improves the quality of the SOI layer due to a reclaimed silicon crystal lattice.

2.4.3 BESOI process

The bonding and etch-back SOI (BESOI) [13] process is used for a mechanically grinding procedure, to lap and polish one of the two wafers to obtain a desired SOI layer thickness (Fig. 2.7). The etch stop is performed by implanting a high dose of boron to introduce a buried oxide. First the wafers are bonded due to van der Waals forces, followed by mechanical wafer thinning and selective etching. The selective etching stops at the boron rich region. The etching of this doped area leads to a better uniformity than mechanical thinning alone. BESOI is limited to films thicker than 5 µm.

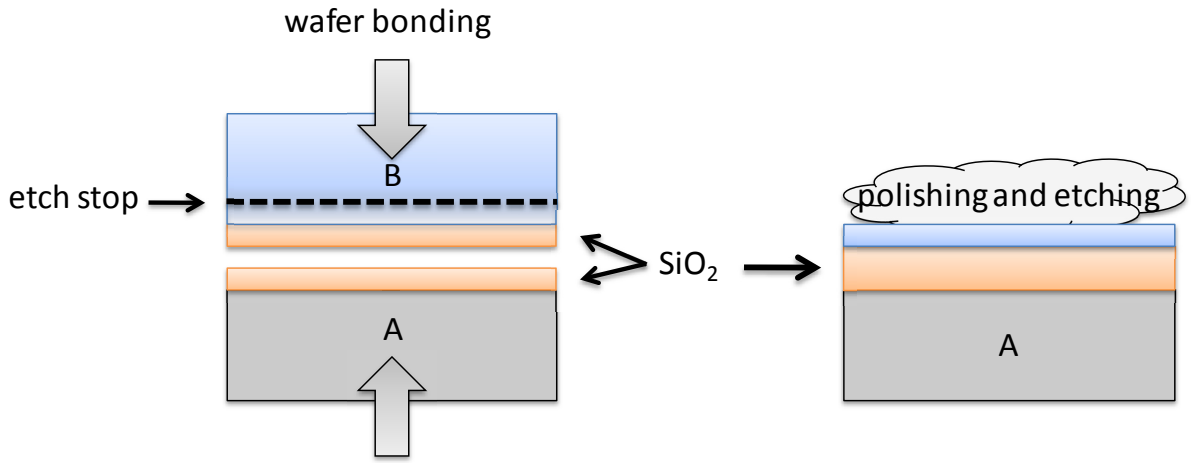


Fig. 2.7 Scheme of the BESOI process.[5]

[5] modified from J. Mähliß, Development of Chromium(VI)-free Defect Etching Solutions for Application on Silicon Substrates

2.4.4 Smart-Cut™ process

Fig. 2.8 shows a schematic presentation of the Smart-Cut™ process [16-19]:

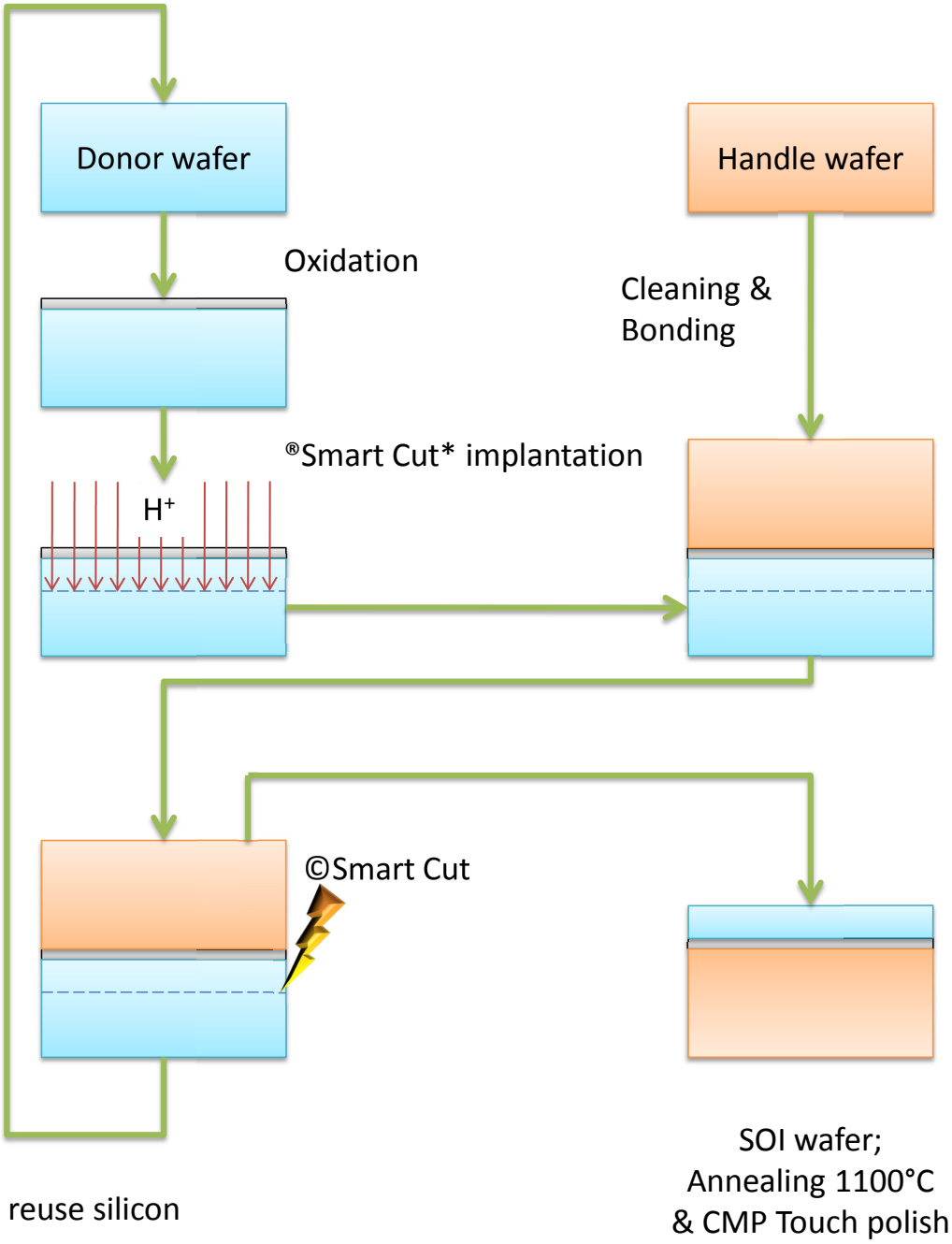


Fig. 2.8 Scheme of the Smart – Cut™ process for SOI manufacturing.[6]

[6] modified from G. Celler, Smart Cut, A guide to the technology, the process, the products, SOITEC (2003)

First, one of the two involved silicon wafers is thermally oxidized to obtain the buried oxide layer. The next step is the implantation of the hydrogen ions with a dose around 2×10^{16} - 10^{17} cm^2 below the oxide layer. The kinetic energy of the hydrogen ions determines the depth of penetration. After cleaning and polishing of the two wafers used, chemical bonding occurs due to van der Waals forces. Van der Waals forces are based on polarisability of atoms or molecules on two material faces being proximal to each other. The two hydrophilic silicon wafers are held together by hydrogen bridges and water molecules. Thermal annealing follows at temperatures around 400–600 °C. The water is lost by diffusion and bonding proceeds as follows:

$$Si\text{-}OH + HO\text{-}Si \rightarrow Si\text{-}O\text{-}Si + H_2O\uparrow$$

The water formed causes further oxidation of silicon, the Si-H bonds dissociate and hydrogen delivers. Micro cavities are formed and separation into a SOI and a silicon wafer occurs due to a cleavage plane. The silicon wafer is used for a further Smart-Cut process. The SOI wafer is annealed at 1 100 °C to reach a full closure of the interface by coupling of the residual interface hydroxyl species. Subsequently the SOI wafer is both cleaned and polished by oxidation and HF treatment.

An advantage of this SOI manufacturing method is its possibility to vary the SOI layer thickness.

2.4.5 Smarter-Cut™ process

The silicon wafer is implanted first with boron ions and subsequently with hydrogen ions. Boron improves the diffusivity and the condensation of the hydrogen used. The annealing temperature decreases up to 200 °C. This procedure enables more variability of the materials used for bonding.

2.4.6 Strained Silicon On Insulator (sSOI)

The idea to develop strained Silicon On Insulator (sSOI) is based on the request for more space between the atoms in the plane of the silicon wafer compared to regular silicon in SOI [20-22] (Fig. 2.9 and Fig. 2.10). An improvement of the electron and hole mobility (up to 70-80%) is reached by the biaxial deformation of the crystal lattice due to the modification of the electronic band structure. The movement of the electrons and holes through the circuit is faster, yielding an improved device performance [23].

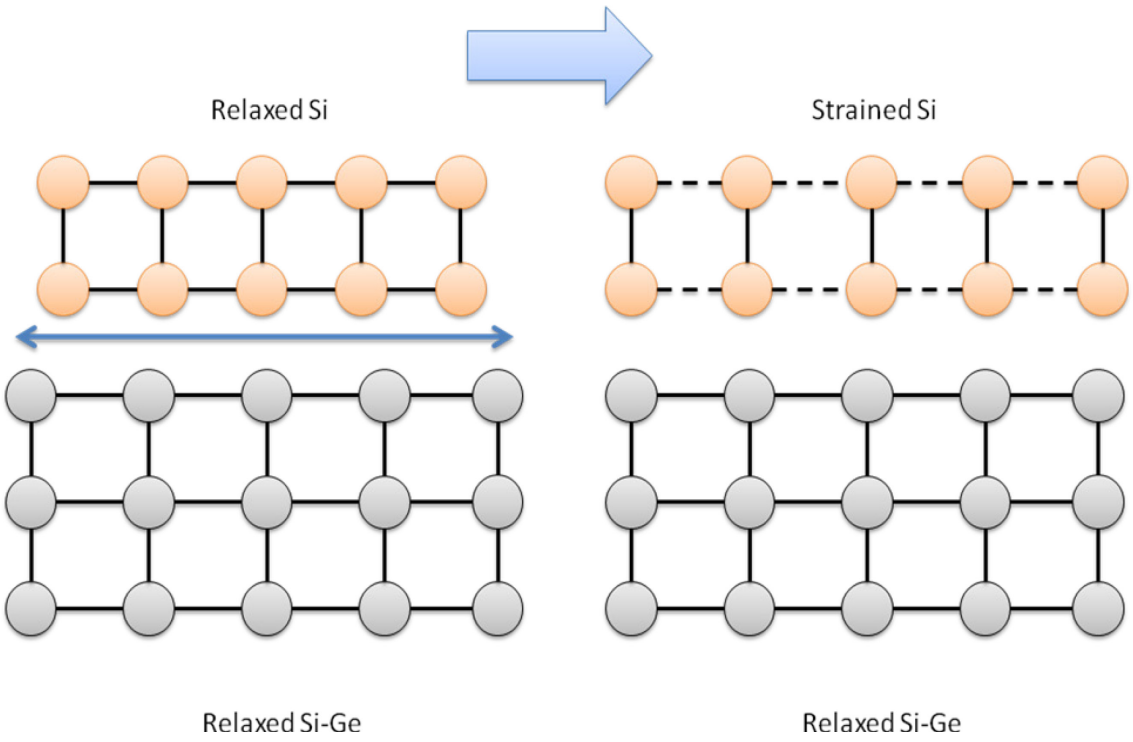


Fig. 2.9 Scheme of the epitaxial formation of sSOI. The SiGe lattice (grey) expand the silicon lattice (orange). When the Si layer (top) overgrows the Si-Ge-buffer layer (center), the lattice expansion remains.[7]

[7] modified from New Ideas for New Materials: Advanced Substrates and Devices for Nanoscale CMOS

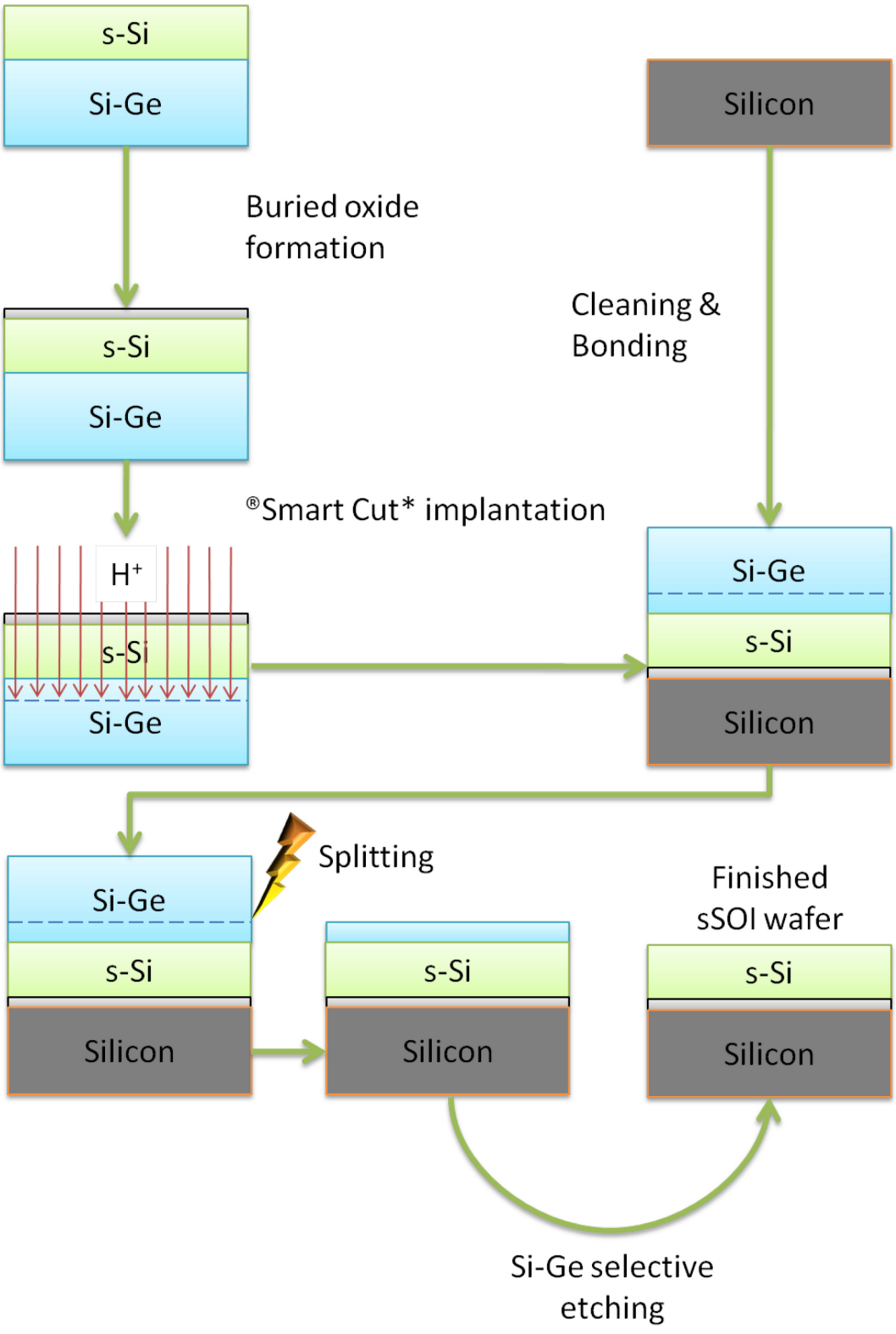


Fig. 2.10 Scheme of the Smart – Cut™ process for sSOI manufacturing.[8]

[8] Modified from G. Celler, Strained Silicon on Insulator, A quick guide to the technology, the processes, the products, SOITEC (2006) and G. Celler, Smart Cut, A quick guide to the technology, the processes, the products, SOITEC (2003)

2.5 Crystal defects

Silicon fabricated for microelectronic applications offers the most perfect crystal lattice manufactured in materials. However, this nearly perfect material contains still different crystal defects which arise during the growth process via CZ or FZ ("Bulk Micro Defects (BMDs)") [24-26]. Imperfections such as vacancy agglomerates (D-defects), interstitial agglomerates (dislocation loops, so-called A-defects), oxygen precipitates, etc. can be explored in such silicon materials [6, 27-30].

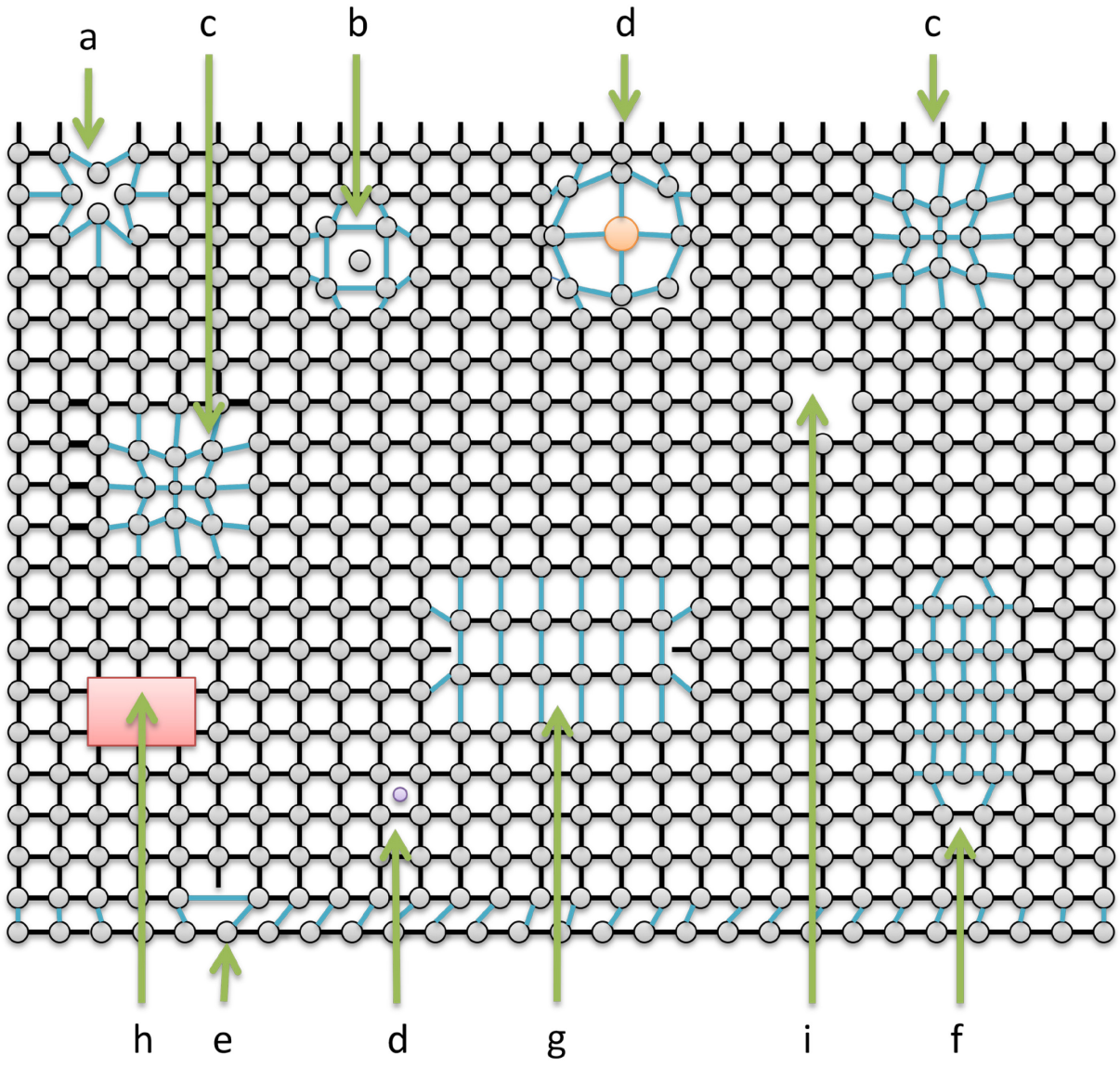


Fig. 2.11 Model of a crystal lattice including different types of crystal defects.[9]

[9] modified from H. Föll, Lecture at the University of Kiel and A. Shimura Semiconductor Silicon Crystal Technology

Fig. 2.11 illustrates several types of defects [31] which can be detected in a crystal lattice as follows:

a. Vacancy: lack of one atom
b. Self-interstitial: addition of a similar atom
c. Extrinsic substitutional atom: expansion or contraction of the crystal lattice
d. Like b. (self-interstitial) with an interstitial impurity atom (coloured)
e. Edge dislocation
f. Dislocation loop due to agglomeration of self interstitials (A-defect)
g. Dislocation loop originated from agglomeration of vacancies
h. Precipitate of impurity atoms
i. Vacancy cluster: voids (D-defects)

Crystal defects are formed by crystal pulling of single-crystal silicon for the wafer manufacturing. They affect the properties of the crystal lattice and consequently the quality of the silicon wafers for microelectronic devices. Defects are a drawback because they:

- Create energy states in the bandgap
- Cause minority carriers
- Decrease the carrier lifetime
- Act as sinks for impurity atoms, in particular metals. These enhance the harmful electronic effects of crystal defects

Crystal defects are classified by their geometry and are illustrated in Tab. 2.1:

Tab. 2.1 Different crystal defects classified by their geometry.

Point defects	Line defects	Plane defects	Volume defects
Intrinsic [29]:	**Dislocations**		
- Vacancy	- Edge dislocation	- Stacking fault	- Precipitate
- Self-interstitial		(extrinsic, intrinsic)	
	- Screw dislocation		- Void (vacancy
Extrinsic:		- Grain boundary	agglomerates)
- Substitutional impurity atom	- Dislocation loop		
- Interstitial impurity atom	(extrinsic, intrinsic)	- Twin	

2.5.1 Line defects

Dislocations are classified as line defects. These are one-dimensional crystal defects which in silicon technology are caused by:

- Mechanical stresses which arise, e.g., by large temperature gradients during silicon crystal growth from the melt or in furnace processes of device manufacturing
- Agglomeration of atomic point defects resulting in the formation of dislocation loops such as A-defects in silicon

The crystal reduces induced mechanical stress by generation of dislocations. This results in plastic deformation of the crystal lattice. Two primary types of dislocations are discussed:

- Edge dislocations (Fig. 2.12)
- Screw dislocations

Normally dislocations result as a mixture of both types of dislocation.

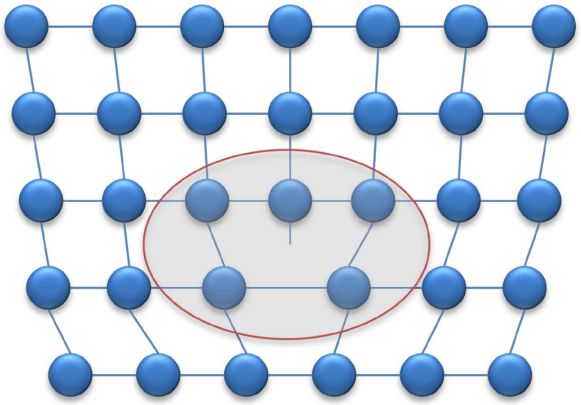


Fig. 2.12 Scheme of an edge dislocation caused by the addition of an extra half plane of atoms in the crystal lattice.[10]

Characterisation of dislocations occurs via their dislocation line and the Burger´s vector b. The insertion of an extra atomic or ionic half-plane into the crystal structure leads to the formation of a dislocation with a dislocation line at the end of the half-plane. The lattice undergoes the strongest deformation at the dislocation line.

The Burger´s vector b is defined by the Burger´s circuit. Normally, in the perfect lattice the starting point and the end of this circuit are identical while surrounding a dislocation the starting and end points of the Burger´s circuit vary (Fig. 2.13). The Burger´s vector completes the circuit. An edge dislocation exists when the Burger´s vector is perpendicular to the

[10] modified from IFW Dresden

dislocation line while the screw dislocation is defined by a parallel position of both Burger´s vector and dislocation line.

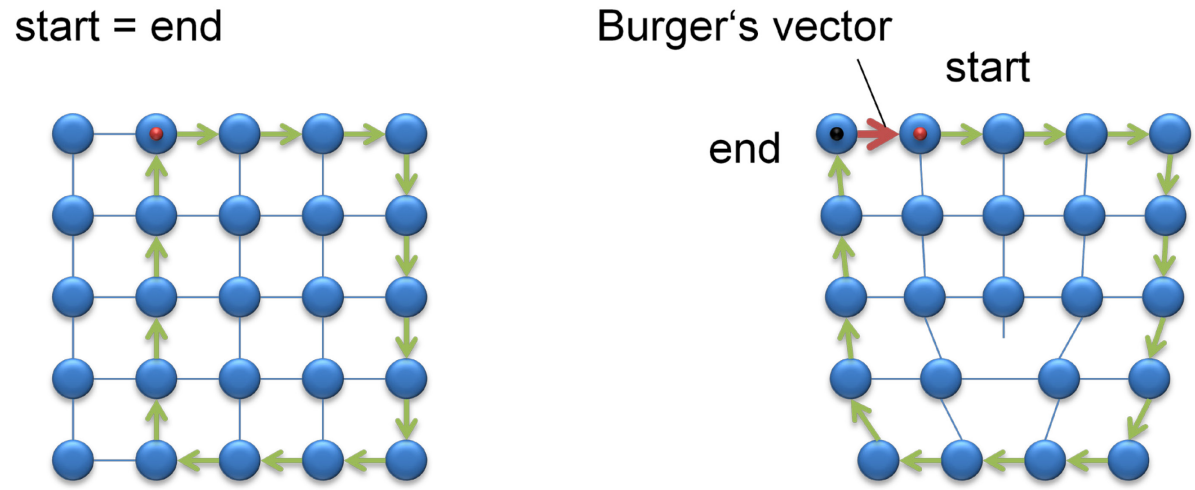


Fig. 2.13 Scheme of the Burger´s circuit in a screw dislocation.[11]

The movement of an edge dislocation through the crystal lattice is shown in Fig. 2.14 from its initiation to the disappearance.

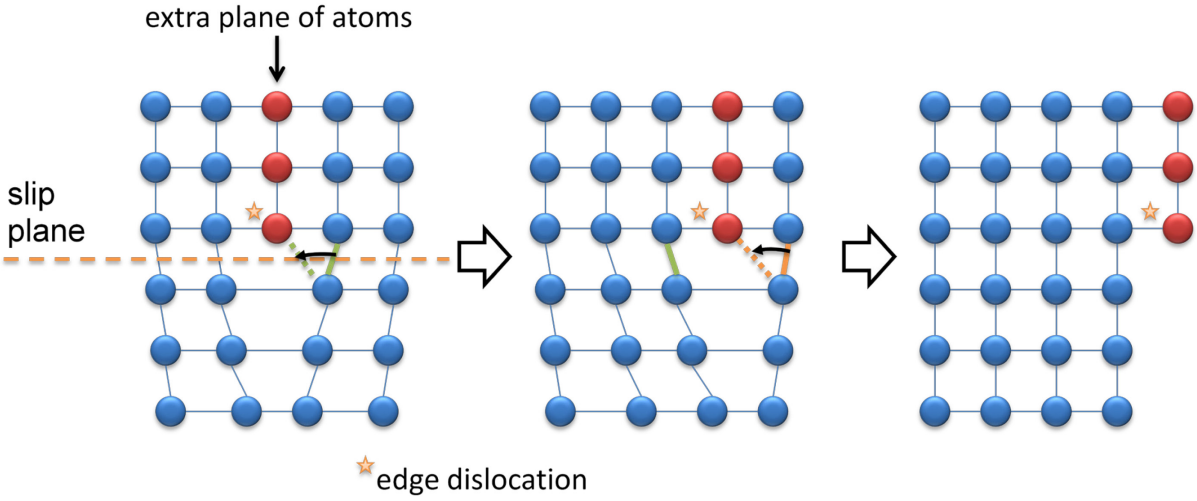


Fig. 2.14 Scheme of the movement of an edge dislocation through the crystal. A row of bonds breaks and reconnects itself to a different row of atoms.[12]

[11] modified from http://www.mrl.uscb.edu

[12] Modified from http://www.ic.arizona.edu/ic/mse257/class_notes/disclocation.html

2.5.2 Plane defects

Plane defects are two-dimensional and can be classified as follows:

- Stacking faults
- Twins
- Grain boundaries

Stacking Faults

The stacking faults (SF) are the most common plane defects in silicon crystals which occur normally in close-packed {111} plane structures. The silicon lattice is a face centered cubic type Bravais lattice (fcc) with an atomic layer sequence of ABC. If an additional lattice plane is added the original sequence of ABCABC is perturbed and becomes ABACABC. This effect is called stacking fault. The lattice vector is defined by d = / ABCA /. The stacking fault perturbs the silicon lattice by b = / BA / = 1/3 d, therefore, the Burger's vector b is in this case just a partial lattice vector. In consequence, the stacking fault is surrounded by a so called partial dislocation.

Oxygen precipitates

Both crystal pulling methods which are used for the preparation of silicon single crystals cause the existence of oxygen in the silicon crystal lattice [32]. The oxygen content is higher in CZ material (10^{18} atoms/cm^3) compared to the FZ material (10^{16} atoms/cm^3).

Fig. 2.15 shows an oxygen atom which is embedded as an interstitial into a silicon crystal lattice. The interstitial oxygen atom O_i is located around the bond axis between two neighboring silicon atoms in the {111} direction forming an angle (Si-O-Si) of 160°.

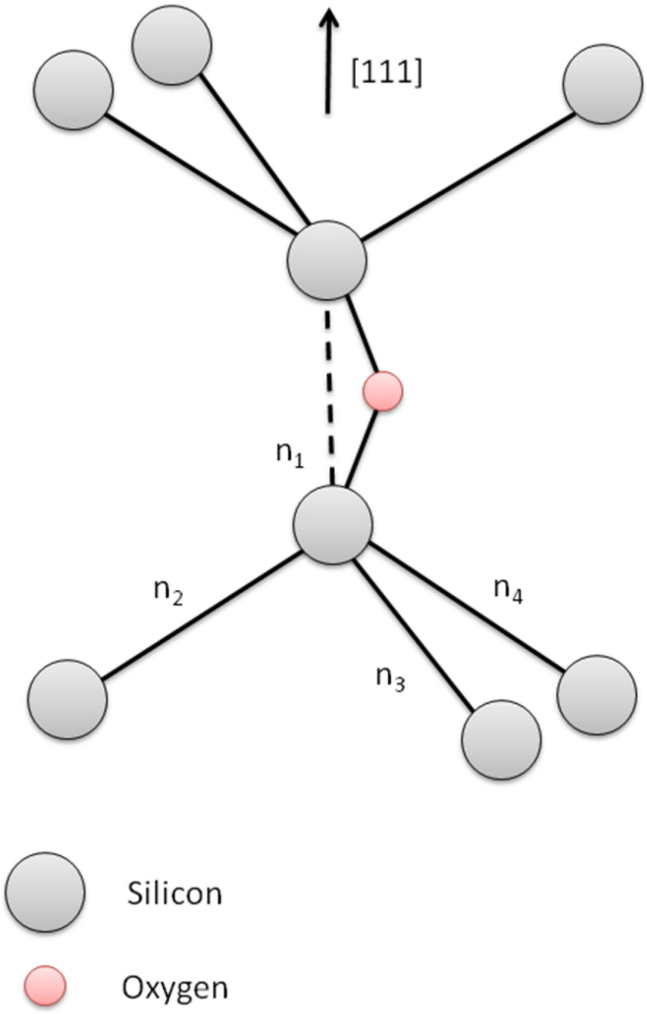


Fig. 2.15 An oxygen interstitial atom embedded in the silicon crystal lattice.[13]

Oxidation induced stacking faults (OiSF/OSF)

OiSF rings are annular rings which offer a high density of oxidation-induced stacking faults (OiSF or OSF) [33, 34].They can be formed in CZ silicon wafers by an annealing procedure at high temperatures of more than 1 150 °C under an oxygen atmosphere. OiSF are formed in the oxidation of silicon by agglomeration of excess Si-selfinterstitial atoms, which are generated at the silicon/silicondioxide interface.

Both the crystal growth rate V and the temperature gradient G influence the actual ring radius. The thermal process triggers the growth of the OiSF which in consequence grow simultaneously resulting in almost similar length of the OiSF.

[13] modified from R. C. Newman, *J. Phys. Condens. Matter* (12), 2000

2.5.3 Volume defects

Volume defects are three-dimensional defects such as precipitates, voids and vacancy agglomerates in crystals.

Precipitates

Precipitates are formed in the crystal lattice when the concentration of impurities exceeds the solid solubility limit. Typical precipitates are silicides caused by metal impurities and silicon oxides caused by oxygen. The rate of precipitation is influenced by the temperature, the diffusivity of the impurity and the degree of supersaturation.

Voids

Voids (D-defects, COPs) are grown-in defects which have their origin in the aggregation of vacancies in silicon crystals [35, 36]. The concentration of vacancies in a crystal is dependent on V/G where V is the growth rate and G the axial temperature gradient at the crystal-melt interface. The variation of V/G in a CZ silicon crystal and a distribution of defects from the center to the edge area in a crystal are shown in Fig. 2.16.

The density of voids is determined by the cooling rate after crystallization procedure at higher temperatures of about 1 100 °C. Voids form typically a polyhedral structure.

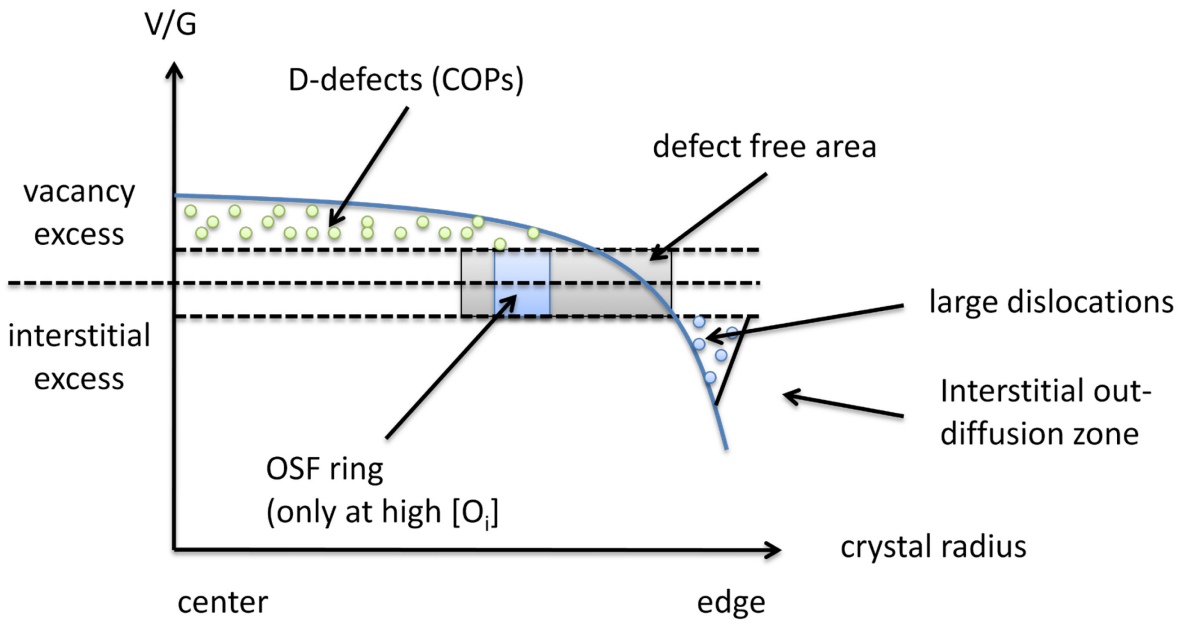


Fig. 2.16 Variation of V/G in a CZ silicon crystal grown. A distribution of defects is shown from the center to the edge area in a crystal. COPs: Crystal-originated particles.

2.6 Wet chemical etching

The wet chemical etching procedure is a simple and reliable method for quality control of semiconductor materials [37-40]. Crystal defects in silicon wafers can be delineated by chemically etching the surface [41-44]. Common crystal defect types are dislocations, swirl defects and vacancy agglomerations. Stacking faults are prominent in sSOI and known in SOI but not common in conventional wafer materials. Defect characterisation occurs using optical light microscopy, scanning electron microscopy (SEM), atomic force microscopy (AFM) or transmission electron microscopy (TEM).

In summary, the application of etching solutions can be classified in four categories:

- Cleaning the surface of semiconductor materials for the removal of impurities
- Delineation of crystal defects in semiconductor materials for quality control
- Determination of the crystal orientation
- Obtaining characteristic properties of the surface

Several etching solutions are well-established which are routinely used for defect delineation in silicon wafers. Etching solutions in general consist of at least one oxidizing and one oxide-solving component. The composition of etching solutions can be classified as follows:

- An oxidizing component: usually a Cr(VI) species or nitric acid to oxidize Si to SiO_2
- A fluoride agent which is generally HF to dissolve the formed SiO_2
- A diluent such as water or acetic acid
- Several additives such as halogens or Cu^{2+}

The etching process can be described by two reaction steps:

$$(1)\ Si + Ox \rightarrow SiO_2$$

Ox = oxidizing component

$$(2)\ SiO_2 + 4\ HF \rightarrow SiF_4 + 2\ H_2O$$

$$SiF_4 + 2\ HF \rightarrow H_2\ [SiF_6]$$

The formation of SiO_2 after the oxidation of silicon is just a formal step to make the principle of the reaction process clear. The mechanism for the oxidation of silicon using HF/HNO_3 mixtures will be discussed in detail later on.

The removal rate is a typical parameter for the etching process which can be described as follows:

$$r = \Delta d / t_{etch}$$

$$r_m = \Delta m / t_{etch}$$

r	removal rate in nm/s
r_m	removal rate in g/s
Δd	removed silicon thickness
Δm	mass loss
t_{etch}	etching time

The removal rate is controlled by the two parameters

- The concentration of the oxidizing agent and
- The concentration of HF

$$r = k [Ox]^a [HF]^b$$

k	rate coefficient for the etching process which depends on parameters such as temperature, etching solution and material used
a, b	partial orders of the reaction

2.6.1 Parameters which influence the etching process

Several parameters are fundamental for the effect of etching solutions:

- The composition of etching solutions
- The concentration of the components in an etching solution
- The etching temperature
- The pre-treatment of the sample
- The type of conductivity of the semiconductor used
- Additives: e.g., metal ions like Cu^{2+} or Ag^{+}
- Crystal orientation

2.6.2 Classification and characterisation of etching solutions

Wet chemical etching is applied for semiconductor defect analysis and polishing as well as cleaning of wafer surfaces. Etching solutions can be divided into two categories:

- Polishing etchants which are diffusion-controlled

- Structural (selective) etchants which are reaction-controlled

A further classification of structural etchants:

- Preferential
- Non-preferential

The activation energy (E_a) is a parameter used for the characterisation of etching solutions which is defined as follows:

$$\ln r = \ln A - E_a / RT$$

r	removal rate
A	pre-exponential factor
E_a	activation energy of the complete etching process
R	gas-law constant = 8.314 $JK^{-1}mol^{-1}$
T	temperature (K)

The activation energy of an etching process is determined by:

1) Measuring the removal rate r of the etching solution at different temperatures
2) Plot ln r against 1 / T
3) Evaluate E_a from the slope

Etching solutions can also be classified by means of the activation energy:

- E_a < 15 kJ/mol: mainly diffusion-controlled etching mechanism
- $E_a \geq$ 15 kJ/mol: mainly reaction-controlled etching mechanism

2.6.2.1 Diffusion-controlled polishing etching solutions

Polishing etchants are applied for the removal of damages and roughness on surfaces of semiconductors. They succeed according to the principle to attack especially particles at and elevated areas of the crystal surface. Due to their uniform removal no etch pits are formed. This means defect delineation does not occur using this kind of etching solutions. High removal rates and low activation energies are characteristic for their etching process. However, a polishing etch can change to a reaction-controlled etch under certain conditions, e.g., change of temperature, composition etc.

A commonly applied polishing etching solution is the CP4 (see appendix 6.1 and chapter 3.8.2).

2.6.2.2 Reaction-controlled structural etching solutions

Structural etching solutions produce etch figures, normally etch pits, at crystal defects such as dislocations, vacancy agglomerates or stacking faults during the preferential etching process.

These etchants exploit the higher local stress leves at defect sites compared to the perfect silicon crystal lattic which accelerates the etching process at these locations through its influence on the activation energy of the etching process.

Fig. 2.17 shows a schematic presentation of the difference in activation energies for a non-decorated defect (E_a^D), a copper decorated defect ($E_a^{D, Cu}$) and the perfect silicon lattice (E_a^P). Mechanical strain caused by crystal defects leads to lower activation energy for the etching process which results in an increase of the removal rate.

Copper decoration of crystal defects is used for the enhanced delineation of even small defects which are scarcely revealed by etching alone. The copper decoration of the defects produces an additional strain in the silicon crystal compared to non-decorated defects which results in further reduction of the activation energy and hence, increased selectivity and an additional increase of the removal rate. Copper decoration will be discussed in detail later on.

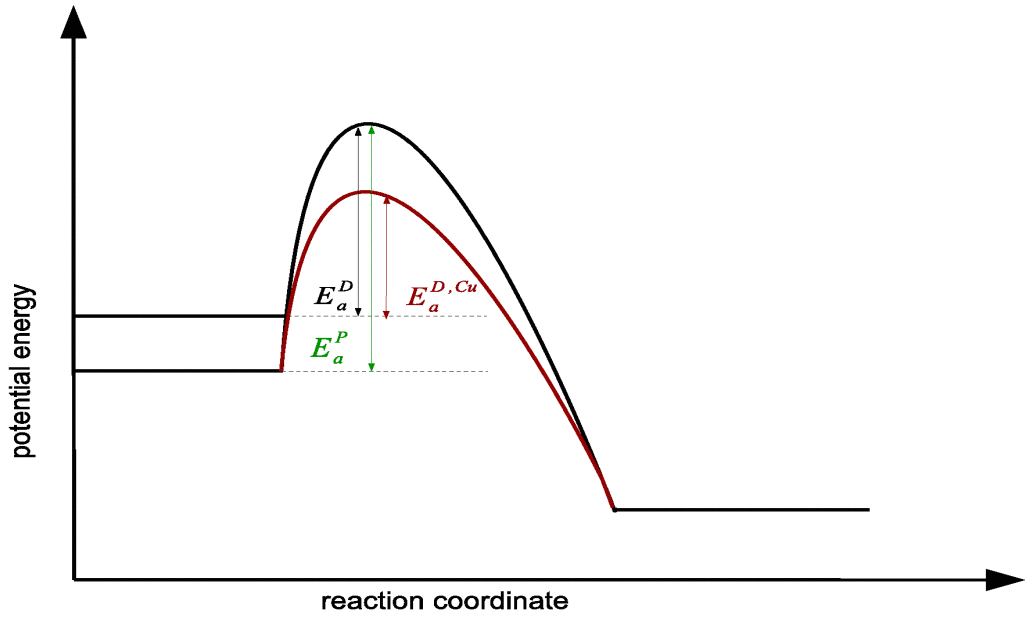


Fig. 2.17 Scheme of the difference in activation energies for a) the perfect silicon lattice (E_a^P), b) a non-decorated defect (E_a^D), c) a copper decorated defect (E_a^D, Cu).

2.6.3 Pit formation

Crystal defects such as dislocations or vacancy agglomerates are the cause of the formation of typical etch pits during the etching process [37]. Pyramidal and alternatively further triangular or square-shaped etch figures are formed by the use of preferential etching solutions on (100) – and (111) – crystal silicon surfaces originating from point–like micro defects, vacancy agglomerates (COPs) or oxygen precipitates.

For etching with a non-preferential etchant the crystal orientation of the material used is not crucial. The etch pits formed normally show a round morphology in horizontal cross-section (Fig. 2.18). A preferential-etching solution leads to the formation of pits with a crystallographic regularity. This is caused by a highly orientation-dependent etch rate. The difference between the vertical etch rate and the directions of the minimum etch rate in the horizontal plane define the planes of the pit surfaces.

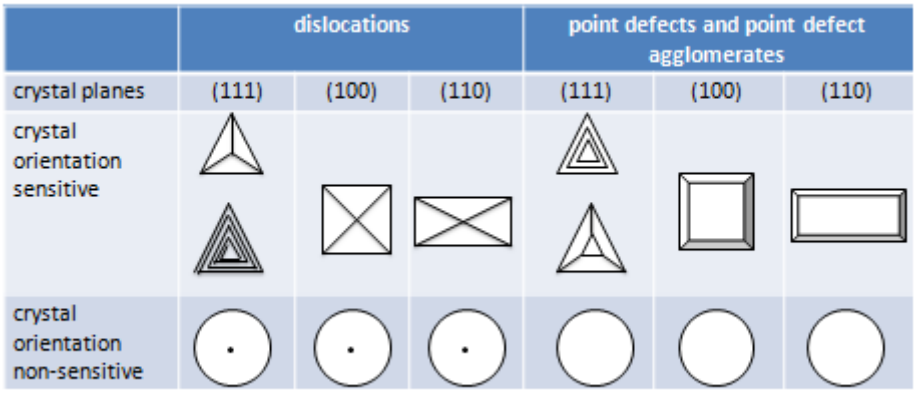


Fig. 2.18 Illustration of the defect type and the crystallographic orientation of etch pits.[14]

2.6.3.1 Preferential etching solutions

The removal is composed of four kinds of partial removal rates using preferential etching solutions (Fig. 2.19):

C_1 removal rate at the perfect crystal orthogonal to the crystal surface

C_2 removal rate at the perfect crystal parallel to the crystal surface

C_3 removal rate at the crystal face ($C_3 > C_1, C_2$)

[14] modified from A. F. Bogenschütz, Ätzpraxis für Halbleiter, Hanser, München (1967)

C_4 removal rate at the crystal defect ($C_4 > C_3$)

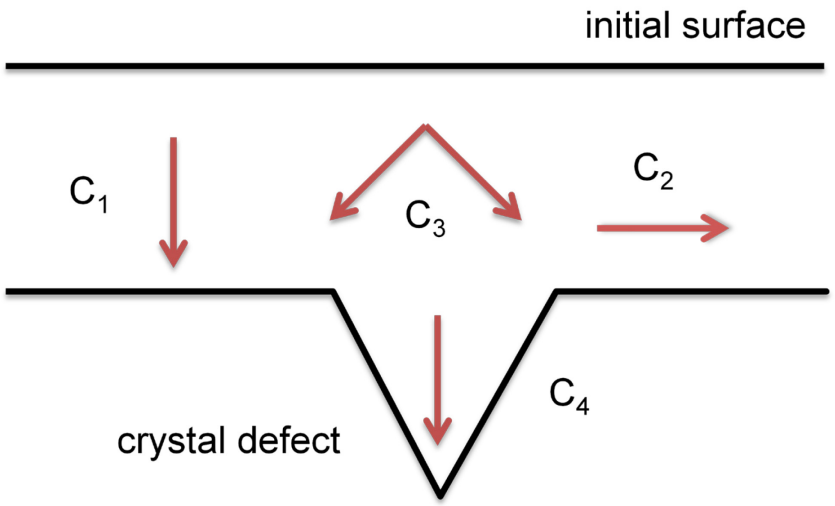


Fig. 2.19 Preferential etching solution: Explanation of the four partial removal rates.

2.6.3.2 Non-preferential etching solutions

The removal is composed of three kinds of partial removal rates using non-preferential etching solutions (Fig. 2.20):

C_1 removal rate at the perfect crystal orthogonal to the crystal surface

C_2 removal rate at the perfect crystal parallel to the crystal surface

C_3 removal rate at the crystal defect ($C_3 > C_1, C_2$)

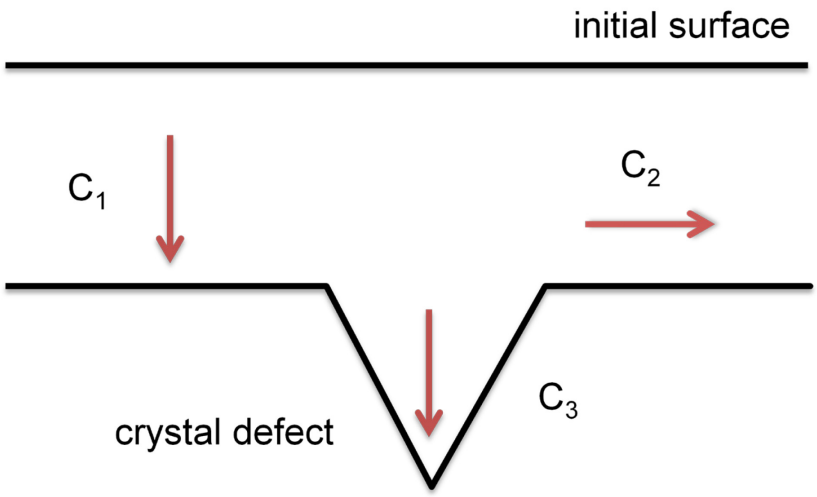


Fig. 2.20 Non-preferential etching solution: Explanation of the three partial removal rates.

2.6.4 Chromium-based etching solutions

2.6.4.1 Secco solution

Most of the structural etches used contain a chromate-species ($K_2Cr_2O_7$ or CrO_3) as the oxidizing agent. The Secco solution (see appendix in section 6.1) was the standard structural etch used for SOI but has been or will be abandoned. Different types of defects can be revealed by etching with a Secco etch:

- Vacancy agglomerates (COPs)
- Stacking faults
- Dislocations in {100} or {111} orientation

The Secco etch works for p- and n-doped silicon in the resistivity range from 4 to 300 Ωcm. It does not etch highly doped material.

Dilute versions of the Secco etch are used for the delineation of crystal defects in thin and very thin SOI films.

The formation of bubbles can be decreased by using ultrasonic agitation during the etching process. These bubbles can induce artefacts at the crystal surface.

The Secco solution shows a linear dependence of the removal on etching time. The removal rate originally published by Secco et al. [45] is around 1.5 µm/min. For the delineation of defects in SOI or sSOI material due to the thin films that have to be characterised, it is necessary to decrease the removal rate by using a dilute version of the Secco. Hence, the hydrofluoric acid and the potassium dichromate content are reduced. The removal rate of the

regularly used dilute version Secco 0.04 M (Cr (VI)) etch is about 0.66 nm/s compared to 25 nm/s for the original mixture given above.

The exact mechanism of the oxidation process during etching is still under debate. Different chromium(VI)- species like $Cr_2O_7^{2-}$, $HCr_2O_7^-$ or $H_2Cr_2O_7$ can be detected in acid solutions. A possible etching mechanism for the reduction of chromium(VI)-compounds in acid solutions is shown in Fig. 2.21 and Fig. 2.22. The first step is the adsorption of chromate at the silicon surface (Fig. 2.21). The following step, an electron transfer from the silicon to the chromium(VI)-species (Fig. 2.22), should be the most plausible reaction mechanism.

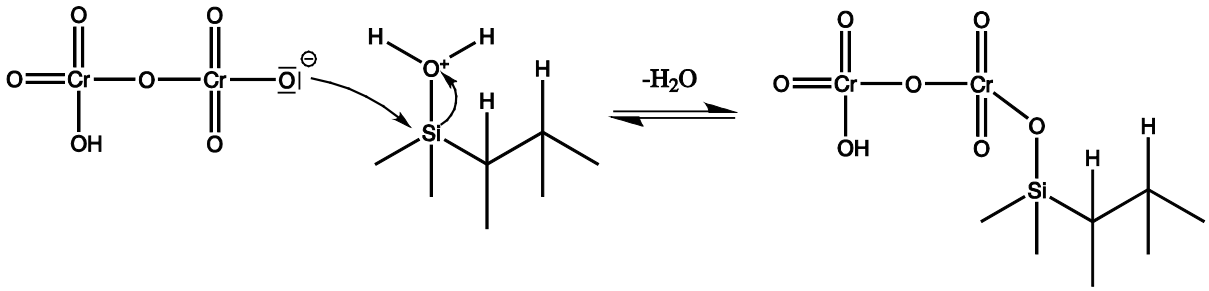


Fig. 2.21 Adsorption of chromate at the silicon surface.

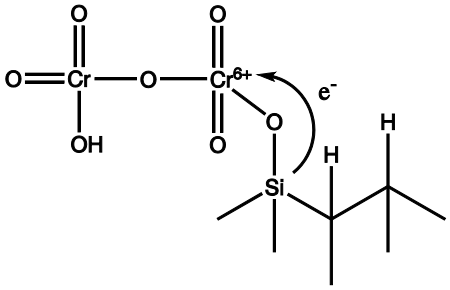


Fig. 2.22 An electron transfer from the silicon to the chromium(VI)-species.

Van den Meerakker and van Vegchel proposed the following alternative etching mechanism:

$$Cr\ (VI) \rightarrow Cr\ (III) + 3\ h^+$$

$$Si + h^+ \rightarrow Si^+$$

$$h^+ = \text{hole}$$

The Cr (VI) compound is reduced by injection of holes into the valance band of the silicon, resulting in the formation of Si^+ species. These quite unstable Si^+ species may be stabilized due to the presence of F^-. Electrons are injected into the conduction band, resulting in the formation of intermediates with higher oxidation states:

$$Si^{+} \rightarrow Si\ (IV) + 3\ e^{-}$$

An electron transfer to protons (H^{+}) in the solution causes the formation of hydrogen:

$$Si^{+} + 3\ H^{+} \rightarrow Si\ (IV) + 3/2\ H_2$$

2.6.4.2 Further chromium-based etching solutions

The compositions of further chromium-based etch recipes are shown in Tab. 2.2.

Tab. 2.2 Compositions of further chromium based etching solutions.

Etching solution	Composition	Removal rate [nm/min], RT
Sirtl	50g CrO_3,100 ml H_2O, 100 ml HF (50%) $[Cr^{6+}]$ = 2.5 mol/l	1 300
Schimmel	7.5g CrO_3,100 ml H_2O, 200 ml HF (50%) $[Cr^{6+}]$ = 0.25 mol/l	1 000
Wright	45g CrO_3, 270 ml H_2O, 6g $CuNO_3$* $3H_2O$, 90 ml HNO_3 (69%), 180 ml HAc (100%), 180 ml HF (50%) $[Cr^{6+}]$ = 0.625 mol/l	1 000

The Wright etching solution [38] can be used to delineate different kinds of stacking faults and so-called bulk micro defects (BMD) in {100} or {111} oriented p- or n-doped silicon crystals. The Schimmel solution is very suitable to reveal crystal defects in Si/Ge materials.

2.6.4.3 Toxicity of chromium (VI)-based solutions

Cr (VI)-species are extremely toxic. Their compounds are unstable in vivo. Cr (VI) is reduced by enzymes to Cr (V), Cr (IV) and finally to the less toxic Cr (III). The toxicity of Cr (VI) compounds lies in its ability to damage cellular components during metabolism. Chronic exposure to dust or vapour of Cr (VI) compounds can affect the respiratory system and cause ulcerations and perforations of the septum, bronchitis and a reduced lung function. The International Agency for Research on Cancer (IARC) has classified Cr (VI) as carcinogenic to humans. $K_2Cr_2O_7$ may also be toxic to the reproductive system and the developing foetus. That is why the handling with Cr (VI) such as $K_2Cr_2O_7$ is already restricted worldwide and chromium-free etching solutions have been developed.

2.6.4.4 Chromium-free etching solutions

Few chromium-free solutions containing HNO_3, HF and HAc are known for the etching of silicon substrates and novel silicon materials such as SOI or sSOI (Tab. 2.3).

Tab. 2.3 Chromium-free etching solutions based on HF, HNO_3, HAc.

Etching solution	Composition	Removal rate [nm/min], RT
Dash	43 ml HNO_3 (69%), 14.5 ml HF (50%), 143 ml HAc (100%)	2.2
FS Cr-free,SOI	95 ml HNO_3 (69%), 12 ml HF (50%), 93 ml HAc (100%) 0.5 ml Br_2 added to 100 ml solution	3.5
Jeita	78 ml HNO_3 (69%), 6 ml HF (50%) 36 ml HAc (100%), 36 ml H_2O	321
MEMC	104 ml HNO_3 (69%), 8 ml HF (50%) 24 ml HAc (100%), 45.6 ml H_2O	469

The Dash [46] solution delineates dislocations and stacking faults in silicon substrates. But the etch figures are poorly developed and have blurred outlines. The etch removal is not uniform and it is unsuitable for SOI and sSOI.

The FS Cr-free etch offers a uniform etch removal with well-formed etch pits [5]. This etching solution can be used for the delineation of crystal defects in standard Smart-Cut^{TM} SOI.

Jeita and MEMC [47] are the most regularly used chromium-free etching solutions for silicon substrates. They are able to reveal D-defects, dislocations or stacking faults. Their etch removal is uniform. However, their etch rates are too high to reveal defects in SOI and sSOI materials.

2.6.4.5 Mechanism of etchants containing HNO_3/HF

Etching samples in HNO_3/HF mixtures are divided in three different steps with NO, $H_2[SiF_6]$ acid and H_2O as the only reaction products:

- *1. Formal oxidation of silicon to SiO_2 by nitric acid*

$$3\ Si + 4\ HNO_3 \rightarrow 3\ SiO_2 + 4\ NO + 2\ H_2O$$

- 2. *Dissolution of the SiO_2 by HF*

$$SiO_2 + 4\ HF \rightarrow SiF_4 + 2\ H_2O$$

- *3.Formation of $H_2[SiF_6]$*

$$SiF_4 + 2\ HF \rightarrow H_2[SiF_6]$$

Overall reaction of the reactions 1-3:

$$3\ Si + 4\ HNO_3 + 18\ HF \rightarrow 3\ H_2[SiF_6] + 4\ NO + 8\ H_2O$$

The detailed mechanism with the oxidation of silicon, being the rate limiting step after Steinert et al., is outlined below:

The silicon surfaces of etched wafer samples were inspected by X-ray-induced photoelectron spectroscopy detecting a Si-H-terminated surface. Steinert et al. proposed a divalent electrochemical dissolution of the silicon (Fig. 2.23-Fig. 2.26). The etching process is initiated by nitric acid inducing holes (h^+) which are located at the silicon surface due to an oxidation process. Subsequently a nucleophilic attack of HF or HF_2^- species at the positively charged silicon surface leads to the formation of Si-F bonds. In the next step polarized Si-Si bonds are attacked by HF or HF_2^- and SiF_4 is formed which reacts with excess hydrofluoric acid to H_2SiF_6 [48].

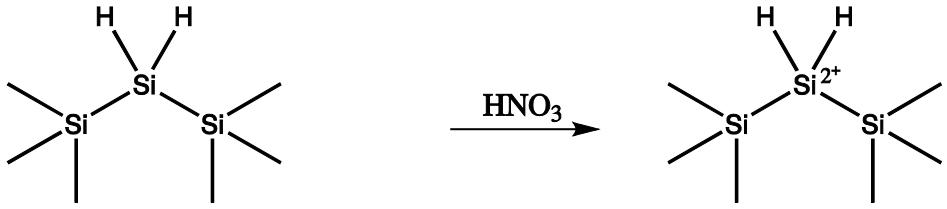


Fig. 2.23 Oxidation of silicon which leads to the formation of holes (h+).

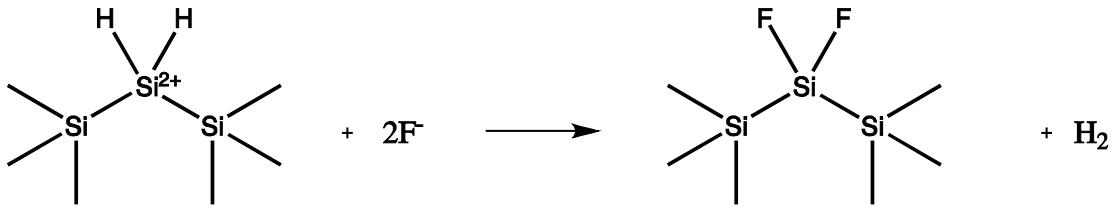


Fig. 2.24 Nucleophilic attack of F- ions resulting in the formation of Si-F bonds.

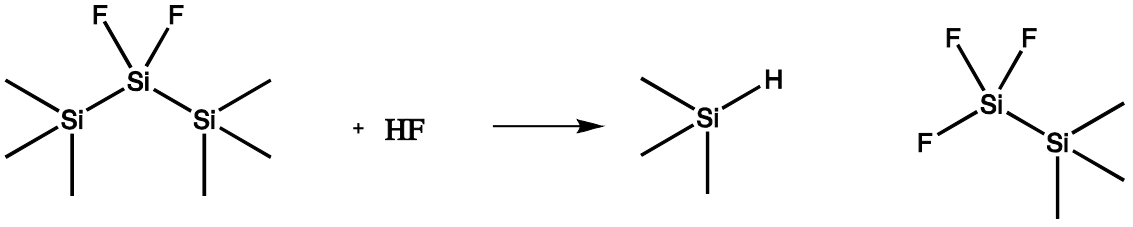


Fig. 2.25 Polarized Si-Si bonds are attacked by HF.

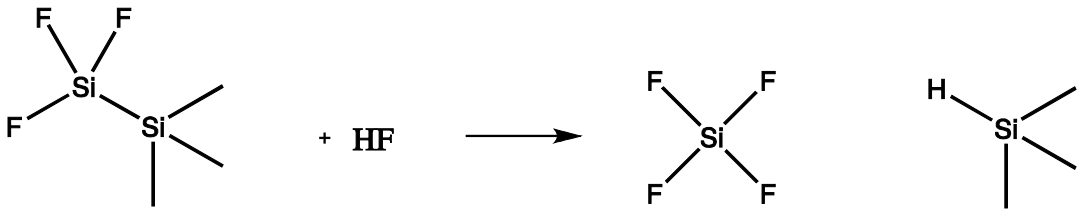


Fig. 2.26 The last step is the formation of SiF_4.

2.7 Analytical methods used

2.7.1 Scanning electron microscopy (SEM)

The scanning electron microscopy (SEM) [49-51] is used for topographic analyses of sample surfaces. Images of both smooth and rough surfaces are taken with low effort due to a high resolution and sharpness. Thereby information of various contrast modes can be obtained simultaneously. Moreover, an energy dispersive X-ray (EDX) detector can be used to determine the chemical elements which are contained in a sample. Following information can be obtained of a sample:

- Topographic structure (secondary electron contrast)
- Material contrast (via backscattered electron contrast)
- Crystal orientation (channeling contrast)
- Magnetic field (magnetic contrast)
- Electrical potential (potential contrast)

A SEM is composed of the following components

- Electron beam-generating system:
  - Cathode
  - Anode
  - Wehnelt cylinder
- Electro-optical system:
  - Two condenser lenses (for the reduction of the electron beam)
  - Objective lens (focusing of electron beam on the sample surface)
- Different detector systems for the backscattered and secondary electron signals
- Vacuum (10^{-3}–10^{-10} mbar)

The sample surface is irradiated with primary electrons (PE) whereby interaction processes induce mainly secondary (SE) and back-scattered electrons (BSE). Furthermore, Auger electrons, X-rays and cathodoluminescence are produced. The SE and BSE are detected by a scintillator-photomultiplier device, resulting in a signal which can be viewed as a digital image.

A high vacuum is necessary for the application of an SEM. Therefore all components of an SEM are located in a vacuum atmosphere. The sample has to be a conductor for successful measurements to avoid negative space charge. Non–conductive samples are sputtered with

a thin gold film to obtain a conductive stage. Semiconductors such as silicon do not necessitate sputtering of a conductive film.

2.7.2 Ellipsometry

Ellipsometry [52, 53] is used for the determination of both the refractive index and the thickness of thin films such as SOI. A schematic presentation of the ellipsometer construction is shown in Fig. 2.27.

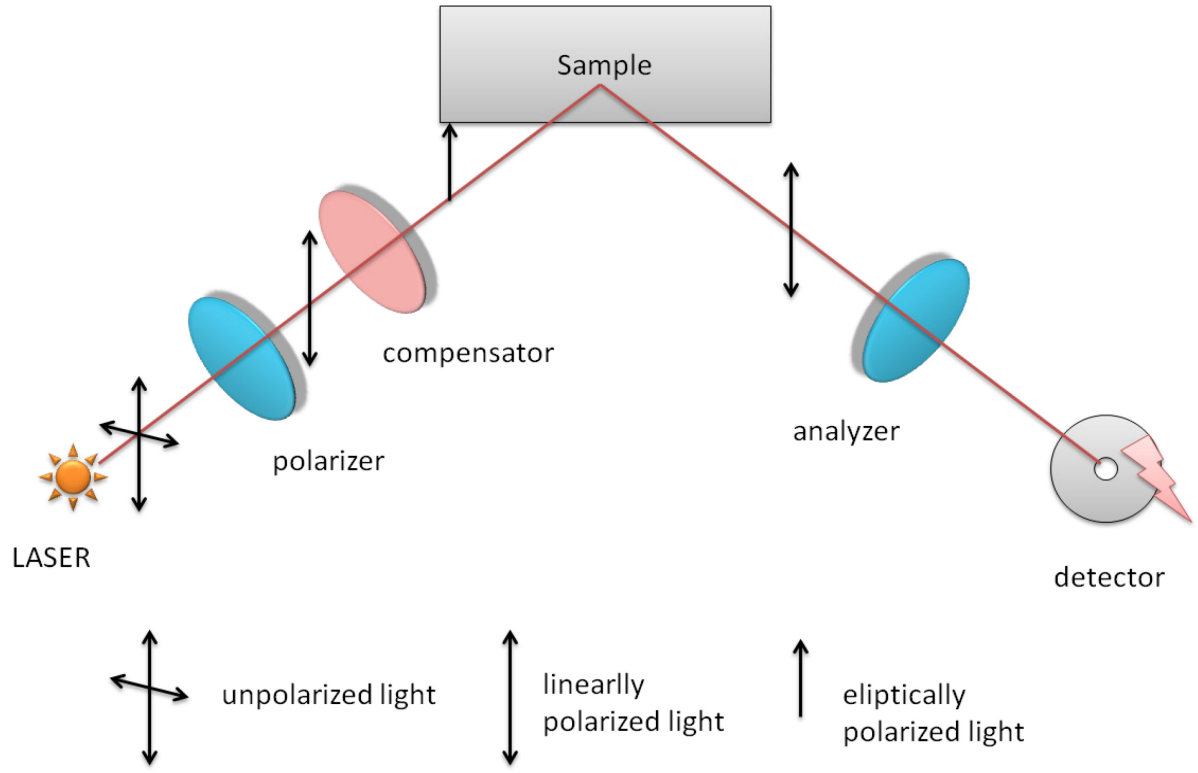


Fig. 2.27 Schematic diagram of an ellipsometer.[15]

An ellipsometer measures the change of polarization upon reflection or transmission, typically in the reflection setup. The exact polarization change is determined by the sample's properties such as layer thickness. Ellipsometry exploits both the phase information and the polarization state of light. It can reach angstrom resolution. This technique is applicable to thin films with thickness less than a nanometer to some micrometers.

The electromagnetic radiation is emitted by a light source such as a laser and then linearly polarized by a polarizer. It can pass through an optional compensator and falls onto the sample. After reflection the radiation passes a second polarizer, the analyzer, and reaches

[15] modified from http://www.scielo.br/scielo.php?pid=S0100-40422002000500015&script=sci_arttext

the detector. The angle of incidence equals the angle of reflection, therefore ellipsometry is a specular optical technique.

2.7.3 Secondary Ion Mass Spectrometry (SIMS)

The secondary ion mass spectrometry (SIMS) [51, 54] is a technique with in-depth resolution for the determination of the detailed elemental components of solid materials. The principle of this method is based on sputtering of a sample with high-energy ions. The bombardment of the sample surface occurs with a primary ion beam containing Ar^+-, Cs^+-, O_2^+-, O^- or Ga^+-ions with a penetration of about 1-10 nm. Thereby both neutral particles as well as positively or negatively charged secondary ions are emitted.

The positively or negatively charged particles are separated and detected due to their mass to charge quotient in the mass analyzer and detector unit of the instrument.

SIMS depth profiles are used for the determination of:

- Doping profiles
- Diffusion profiles
- Isotope ratios of elements

2.7.4 Atomic Force Microscopy (AFM)

The atomic force microscope [55, 56] is a type of a scanning probe microscope which offers a very high resolution. Fig. 2.28 shows a scheme of an AFM.

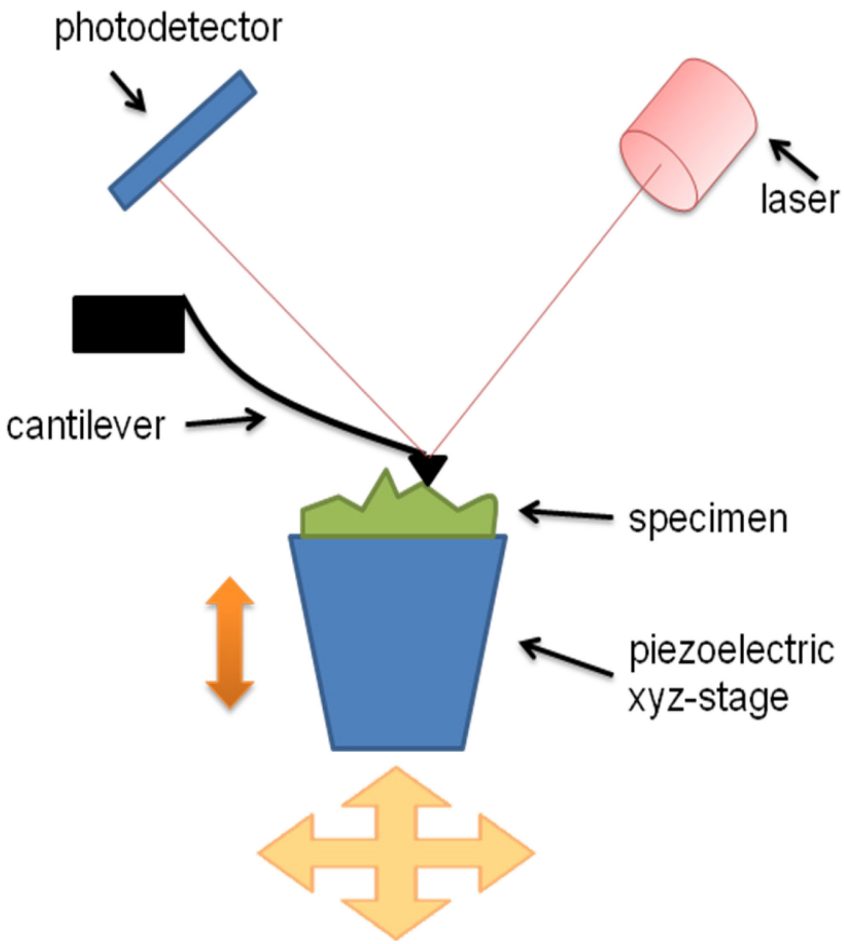


Fig. 2.28 Schematic diagram of an AFM.

The cantilever of an AFM is made of silicon or silicon nitride and equipped with a sharp tip at its end for probing the specimen surface by scanning. The tip radius of curvature is about ten nanometers. When the tip is placed into proximity of the sample surface for an AFM measurement repulsive or attractive forces occur between the tip and the sample. These forces cause a deflection of the cantilever according to Hooke`s Law:

$$\Delta z = \Delta F / k_c$$

Δz	Deflection
ΔF	Acting force
K_c	Spring constant

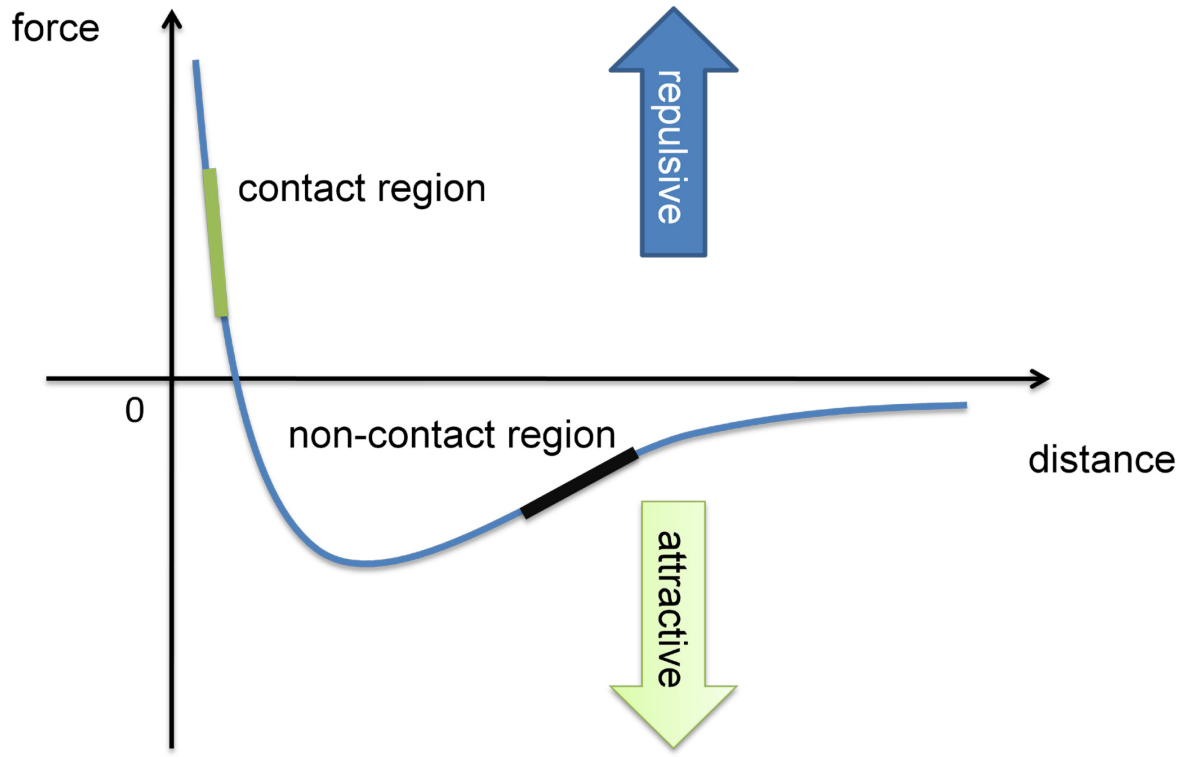


Fig. 2.29 View of the interaction force versus tip-sample distance.

At the very right area of the curve in Fig. 2.29 separation of the atoms of tip and sample corresponds to a large distance with practically no interaction between tip and sample. The attraction by van der Waals forces between the atoms increases when the atoms are approached to each other. The further the atoms approach, the more dominant the Pauli Repulsion force becomes. After the equilibrium distance is reached, further reduction of the distance between tip and sample leads to a repulsion due to the Pauli exclusion principle for their electrons.

2.8 Decoration

Very small crystal defects of a few nanometers in size are scarcely revealed by etching alone. Decoration is a well-established method used to facilitate the detection of such small defects in silicon wafers [46, 57-72]. The precipitation of suitable metals such as copper or lithium occurs preferentially at defects under silicide formation (Cu_3Si, LiSi) [73-79]. These grown-in or process-induced crystal defects act as nucleation sites for the precipitation of metals. The metal deposition leads to the magnification of the defects and improves their delineation after etching. They may be characterized by light optical microscopy and scanning electron microscopy (SEM).

A shortcoming of the decoration method, especially copper decoration, is the tendency of the metal to form artefacts due to precipitation at the silicon wafer surface when the concentration used is too high.

2.8.1 Copper decoration

Copper belongs to the 3d transition metals of the 4th period of the periodic table [80]. Owing to its electron configuration, Cu differs in its properties from the other 3d transition metals. Copper has the irregular electron configuration $3p^6 3d^{10} 4s^1$ instead of the expected electron configuration $3p^6 3d^9 4s^2$. One of the 4s electrons is inside the 3d shell. Copper differs in its behaviour when diffused into silicon from the other 3d transition metals. The ionization of the neutral copper to Cu^+ leads to the stable configuration $3d^{10}$. The small radius of Cu^+ (74 pm) may be attributed to its closed shell. This small Cu^+ is relatively inactive in the silicon lattice.

Both the small radius of copper and its low interaction with the silicon lattice facilitate the high diffusivity of copper in silicon [81, 82]. Hence, diffusion of copper occurs in silicon even at room temperature.

Two models for the electron configuration of copper as interstitial copper in the silicon crystal lattice have been proposed [80]:

- Electron configuration of Cu: $3d^{10} 4s^1$ and of Cu^+: $3d^{10}$. The Cu^+ is inert in the silicon lattice due to its closed shell the copper in the silicon lattice transfers some electrons from the 3d into the 4sp shell. Furthermore, the copper absorbs the electron density of the neighboring atoms. The Cu^+ forms a weak covalent bond with its four surrounding silicon atoms.

Copper is the only 3d metal that forms a Me_3Si compound. This silicide leads to a much larger molecular cell volume in the silicon lattice and a defect magnification occurs.

The properties of copper in silicon can be summarized as follows [83, 84]:

- Positive charge
- Weak interaction with the silicon lattice
- Strong expansion of the silicon lattice caused by the formation of the copper silicide (Cu_3Si)

The extremely high diffusivity of copper is about 2.8 x 10^{-7} cm^2/s at room temperature due to its small ionic radius and its weak interaction with the silicon lattice. The diffusion barrier for atoms depends on their elastic and electronic interaction with the lattice atoms. The diffusion barrier for copper is about 0.18 eV and consequently lower than that for other metals which diffuse into silicon.

The solubility of copper in silicon is very low, being less than 1 atom/cm^3 at room temperature. However, the solubility increases to about 10^{18} atom/cm^3 at a temperature of 1 000 °C.

The copper decoration of silicon wafers [85-88] occurs via furnace annealing. On cooling, the dissolved copper is deposited at the crystal defects or at the surface of the silicon wafer. Copper could also diffuse out of the wafer when quenched to room temperature. Subsequent reactions caused by the dissolved copper in silicon (Fig. 2.30) are:

- Formation of point defects and their complexes
- Formation and precipitation of copper silicides (“decoration”) at crystal defects such as dislocations in the bulk by heterogeneous nucleation or at the surface via homogeneous nucleation
- Rapid diffusion of the copper to and at the silicon surface
- Precipitation of the copper at the p^+-area

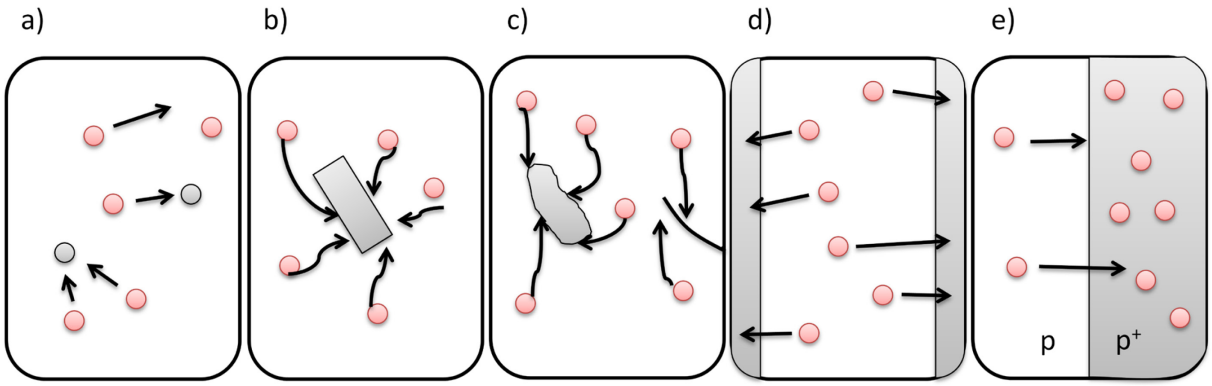


Fig. 2.30 Characteristic reactions of copper in defects in silicon: a) formation of point defects and their complexes; b) silicide formation; c) decoration of defects such as dislocations and grain boundaries; d) diffusion of copper to the silicon surface; e) precipitation at the p+-area (diagram source).[16]

One condition for the deposition of copper in defects is the supersaturation of the silicon with dissolved copper during the cooling step. A particular threshold must be reached for the activation of nucleation and silicide growth. A high cooling rate leads to a higher density of small copper precipitates while a low cooling rate results in a lower density of larger copper precipitates.

Copper precipitation results in an enlargement of the silicon lattice. The atomic volume of silicon is just 20 $Å^3$ compared to the much larger molecular cell volume of a copper silicide moiety Cu_3Si which is 46 $Å^3$.

2.8.2 Lithium decoration

Lithium has the following properties which make it attractive for the decoration procedure [89-95]:

- High mobility in silicon
- Low ionization energy (0.033 eV)
- It is readily ionized
- Small ionic radius (60 pm) facilitates its fast diffusion through the silicon lattice
- Diffusivity: 4.8 x 10^{-11} cm^2/s at 160 °C
- Lithium precipitation is limited by its diffusivity in silicon assumption of silicide formation in silicon: LiSi (much smaller than Cu_3Si)

Lithium decoration of the defects occurs at temperatures as low as 400 °C by diffusion through the silicon wafer. Lithium precipitates in the interstitial sites of the silicon lattice under

[16] modified from Physics of Copper in Silicon, Istratov et al., *J. Electrochem. Soc.*, ***149*** *(2002)*

silicide formation (LiSi). Decoration with lithium has the advantage that it hardly forms artefacts in contrast to copper decoration when the metal concentration used is too high. Copper decoration is superior to lithium decoration due to the simplicity of its practical procedure.

3 Experimental Details

Copper decoration in combination with preferential etching is the procedure that was used for the delineation of crystal defects in SOI and sSOI wafers. The crystal defects were decorated using either with $Cu(NO_3)_2$ - or $LiNO_3$ solutions of varying metal concentrations. Experimental parameters such as concentration and volume of the solution used and annealing temperature for the decoration procedure were developed and optimized.

The preferential etching solutions used were selected according to the type of crystal defect to be delineated (see appendix 6.1 for their compositions). After etching, the wafer fragments received a short dip in a 50% solution of HF. This procedure is used to magnify the defects. The BOX below the defect is etched and appears as a halo around the defect when viewed under the microscope, thus facilitating its detection.

The optimum combinations of solution used and etching time were determined for the decoration.

Defect densities were determined and defects were characterized with a light optical microscope. Selected defects were analysed in a SEM and in an AFM. Several SIMS profiles were made to analyse the decoration process in the SOI fragments.

The SOI and sSOI wafers provided by SOITEC SA/Bernin, France, were cut into squares of ~ 1 cm length and cleaned with blasts of nitrogen. The thicknesses of the SOI and sSOI-films used were about 20-1 400 nm and 14-85 nm respectively.

The thicknesses of the BOX were as follows:

- *Thin SOI:* 10 nm
- *Standard SOI:* 145 nm
- *Thick SOI:* 300 or 1 000 nm
- *sSOI:* 145 nm

3.1 Decoration procedure

Solutions for Cu and Li decoration with concentrations ranging from 0.0001 to 100 ppm were prepared by dilution of a 1 000 ppm $Cu(NO_3)_2$ and $LiNO_3$ standard solution respectively. These were used to decorate the fragments.

Two different decoration methods were used:

- *Copper Decoration via furnace annealing:*
  Fig. 3.1 shows a scheme of the experimental steps of the copper decoration procedure. Decoration was accomplished by pipetting dilute $Cu(NO_3)_2$- or $LiNO_3$-solution of known volume and concentration on the back of the fragments and drying them by heating on a hot plate. The fragments were then annealed in a furnace at a temperature in the range of 800-950 °C for 1 minute after which they were quenched in air to room temperature [96]. The annealing temperature depended on the thickness of the buried oxide (BOX) layer in the SOI fragment (Tab. 3.1):

Tab. 3.1 The annealing temperatures used according to the thicknesses of the BOX layer in the SOI fragment.

LT BOX [nm]	Annealing temperature [°C]
145	800
300	900
1 000	950

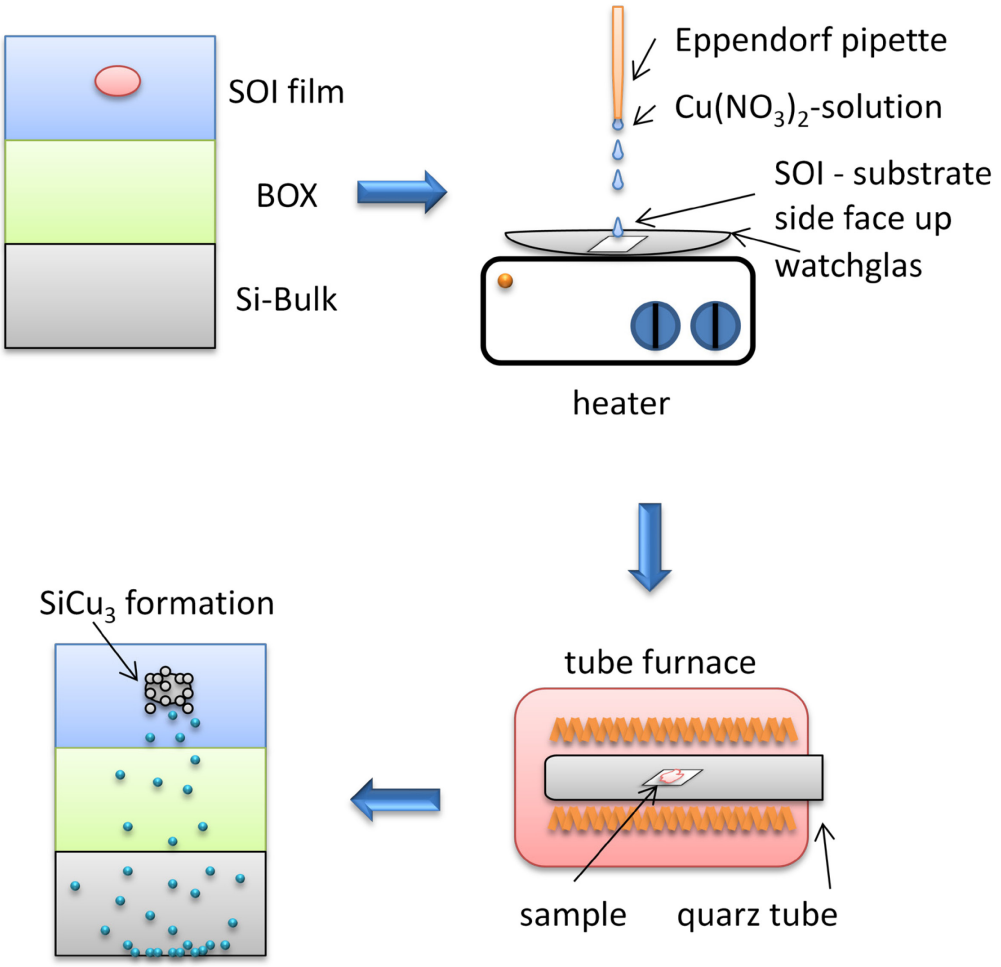


Fig. 3.1 Schematic presentation of the copper decoration process.

- *Electrochemical copper deposition out of a dilute $Cu(NO_3)_2$ spiked hydrofluoric acid solution:*

  The SOI fragments were placed vertically in a Teflon™ sample-holder and dipped for 1 min in a 5% hydrofluoric acid solution containing 0.1-10 ppm of a $Cu(NO_3)_2$ solution. The solution was not stirred. The samples were then rinsed in Millipore water for two minutes and dried with short blasts of nitrogen.

3.2 Etching procedure

After copper or lithium decoration the SOI and sSOI fragments were etched with etching solutions such as dilute Secco (0.04 M Cr (VI)) (Tab. 3.2). The reaction vessels used for preparing and storing the etching solutions – generally about 150 ml - were of polypropylene with a maximum volume of 200 ml. All etching solutions were prepared the day before they were used to stabilize the solution prior to etching.

Most of the etching experiments were carried out at room temperature of 23 °C. Some of the experiments were performed at lower temperatures using a thermostat.

The wafer fragments were placed vertically in a Teflon^{TM} sample holder and immersed in the etching solution for a given time. Wafers of different types were not placed together in the same solution. The solution was not stirred during etching. The fragments were generally etched from their initial layer thickness down to approx. 20-70 nm and rinsed in ultra-clean Millipore water for two minutes. The fragments were then dipped in 50 % HF for approx. 45-90 s to remove the BOX below the etch pits for defect delineation. Subsequently the samples were rinsed in Millipore water for two minutes for quenching. The following etching solutions were used during these studies:

Tab. 3.2 Etching solutions used (for detailed composition see appendix section 6.1).

Etching solution	Application
Dilute Secco (0.04 M Cr (VI)) (HF, $K_2Cr_2O_7$, H_2O)	Standard etching solution for SOI sSOI, but containing Cr (VI)
OPE (different compositions: A,B, D, F) (H_2O_2, HF, HAc)	SOI, sSOI
CP4 (HF, HNO_3, HAc, KIO_3, KIO_3 + KI)	610 nm SOI
CA (Chloranil, Dioxan, HF)	SOI
Jeita Jeita A: (HF, HNO_3, HAc, H_2O), Jeita B: (HF, HNO_3, HAc, H_2O, KI))	1 400 nm SOI

3.3 Defect characterisation

The thicknesses of the silicon layers in the fragments were determined prior to and after etching with an ellipsometer. Some of the thicker SOI film layers had to be measured with a Stylus profilometer as the surface after etching was too rough for accurate measurements with the ellipsometer. The etching times were determined by a stop watch.

Defect densities were routinely determined with the help of a light optical microscope at magnifications of 200–1 000 x in the bright field modus. 10–20 images were taken of each sample surface, the etch pits on each image were counted and the sum divided by the measured area of the corresponding image to give the defect density. The radius of the halo at some etch pits was also measured in each image. The defect densities and radii of the halos of Cu and Li decorated samples were compared with those of non-decorated samples ("references 1") and with those of annealed but non-decorated samples ("references 2").

Selected defects were examined in detail using SEM and AFM. Furthermore some SOI fragments were analysed via SIMS. Fig. 3.2 is a schematic representation of the whole experimental procedure:

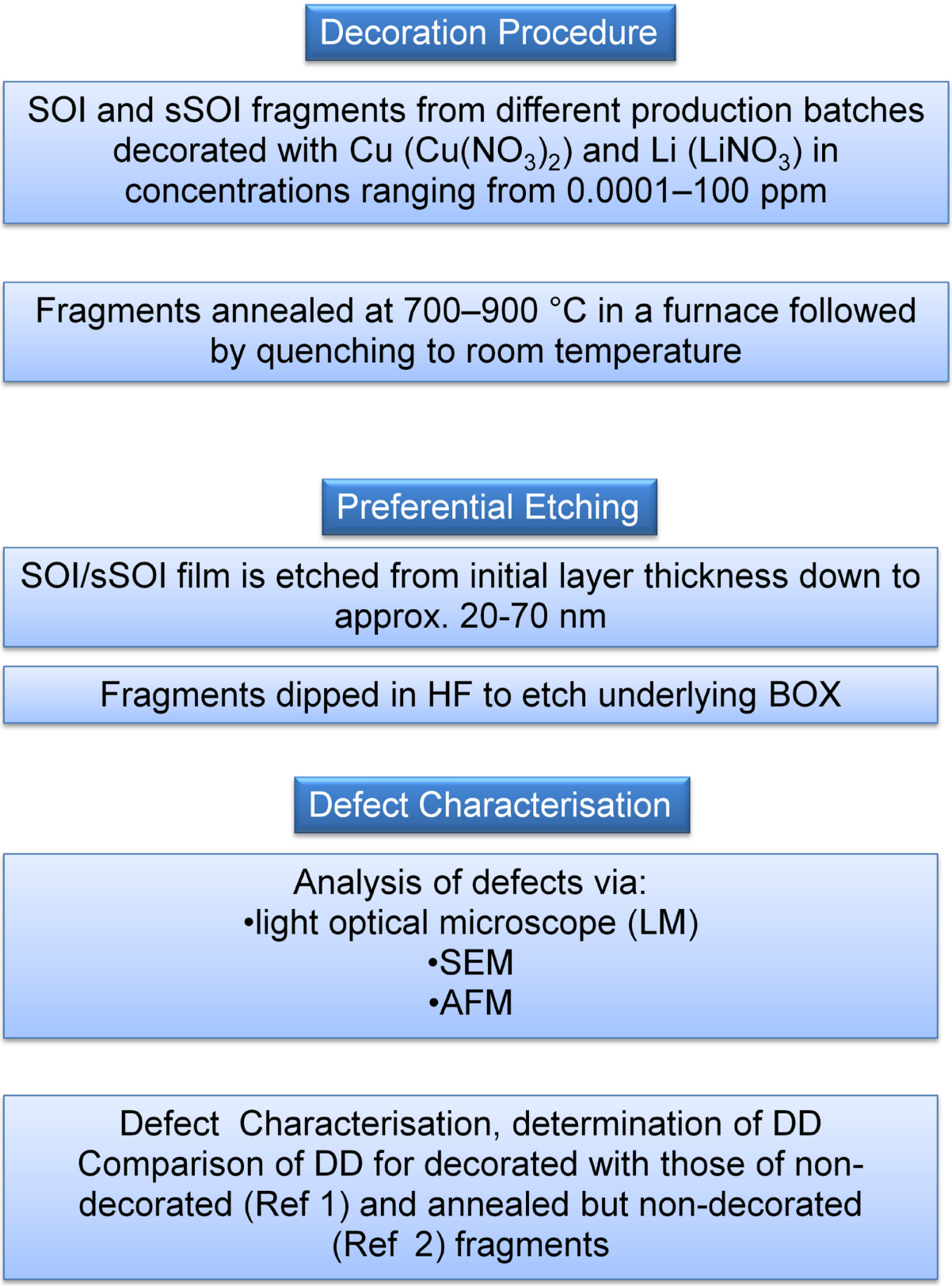


Fig. 3.2 Diagram to give an overview of the experimental procedure. DD: defect density.

The scheme in Fig. 3.3 shows the preferential etching process of a SOI fragment:

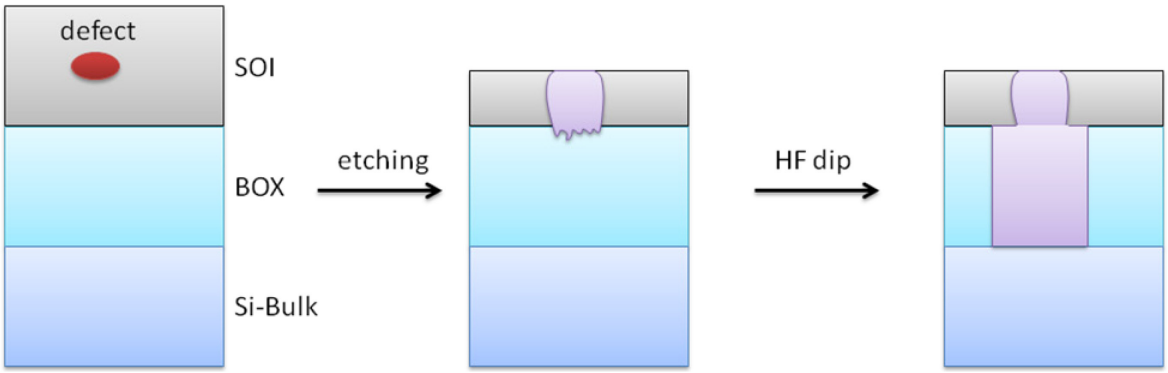


Fig. 3.3 Scheme of the preferential etching process.

3.4 Delineation of crystal defects

Different etching solutions were used for the delineation of crystal defects. All the etching solutions were able to reveal different types of crystal defects.

For the delineation of crystal defects such as COPs or OiSF in SOI and Stacking Faults or Threading Dislocations in sSOI a dilute Secco etch was routinely used. Other etching solutions such as OPE (Organic Peracid Etches) (section 3.10) or Jeita A and B (section 3.8.1) which were chromium-free [97] were also used for defect delineation. Reference samples were non-decorated fragments etched under the same conditions.

Generally the crystal defects which can be revealed in the SOI films investigated are as follows:

- COPs (Crystal Originated Particles) which are vacancy agglomerates (Fig. 3.4)
- "Red spots" which are decorated defects at one of the two interfaces SOI-film/BOX or BOX/Si substrate (reddish dots in Fig. 3.4)
- OiSF (Oxidation-induced Stacking Faults) which are formed in the SOI fabrication process (Fig. 3.4)

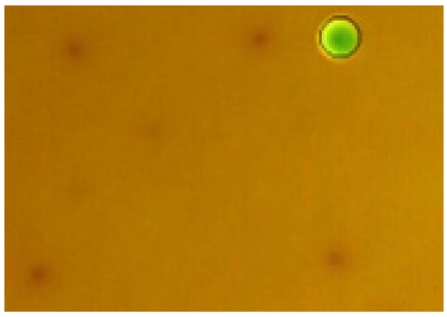
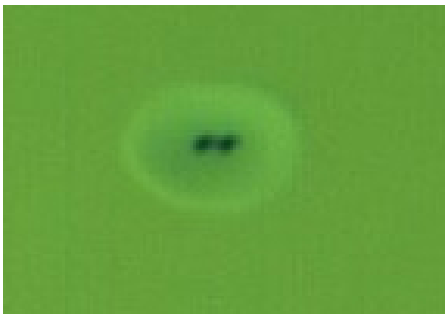
a)  **b)** 

Fig. 3.4 Typical crystal defects in SOI after etching with a dilute Secco (0.04 M Cr(VI)) followed by an HF dip of 45 s: a) One COP (defect is delineated as a circular pit) and "red spots" (red features) visible in a copper decorated fragment, b) OiSF with characteristic connected double dot feature surrounded by a bright oval halo.

The following crystal defects have been delineated in the sSOI film:

- TD (Threading Dislocations) (Fig. 3.5)
- SF (Stacking Faults) (Fig. 3.5)

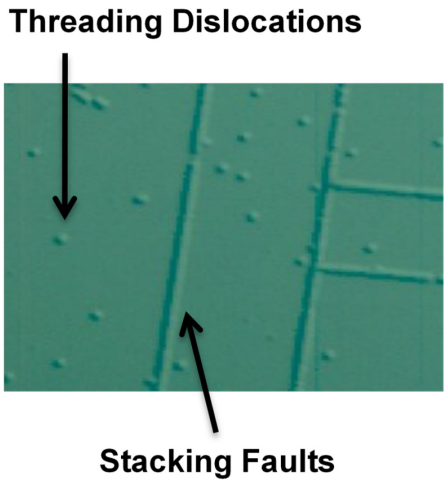


Fig. 3.5 Typical crystal defects in sSOI after Cu decoration and etching with a dilute Secco (0.04 M Cr (VI)).

The crystal defects and their delineation with metal decoration and etching with different mixtures will be discussed in detail later.

3.5 Decoration of crystal defects in silicon materials

3.5.1 Copper decoration

In silicon wafers decoration with metals such as copper enables the detection of small crystal defects which are hardly revealed by etching alone.

The diffusivity of copper in silicon is very high due to its small ionic radius and its weak interaction with the silicon crystal lattice (diffusion coefficient of Cu in Si: 2.8 x 10^{-7} cm^2/s at room temperature). The diffusion barrier is about 0.18 eV for the copper diffusivity in silicon and thus lower than the diffusion barrier of other possible impurities in silicon. Therefore copper is very mobile in silicon and diffuses even at room temperature through the wafer. Furthermore at high temperatures copper is highly soluble in silicon (10^{18} cm^{-3} at 1 000 °C).

When copper dissolves in silicon two main reactions are possible in the subsequent cooling process:

- The copper precipitates in the silicon
- The copper diffuses out of the silicon when the fragment is removed from the furnace

A high cooling rate after copper decoration in a furnace leads to precipitation of copper in crystal defects or in the silicon lattice. Precipitation occurs under formation of the silicide Cu_3Si which occupies a much larger space than silicon. Cu forms a covalent bond with four silicon neighbors under considerable lattice expansion. A low cooling rate causes the out diffusion of copper. In general a rapid cooling leads to a high density of small copper precipitates while slow cooling results in a low density of large precipitates. Heterogeneous nucleation occurs with a lower barrier compared to homogeneous nucleation. Hence, copper decorates crystal defects in the silicon lattice by precipitation. One drawback of copper decoration is its tendency to form artefacts due to copper precipitation at the wafer surface when the copper concentration used is too high. First, all crystal defects present get decorated with copper. Then nucleation of copper occurs at the perfect silicon lattice forming artefacts. This can result in the determination of higher defect densities than appropriate. As the objective of the copper decoration studies was the decoration of different types of crystal defects in silicon wafers the decoration conditions were largely designed to avoid the formation of artefacts and the defect densities of copper decorated silicon fragments were compared with non-decorated reference fragments. Some of the reference samples were just etched with different preferential etching solutions (Ref 1) while others were first annealed in

a furnace and then etched with different etching solutions (Ref 2). The latter was performed to rule out accidental copper cross contamination in the furnace used.

Generally copper decoration was achieved by furnace annealing. Copper cross contamination caused by the annealing procedure in the furnace may lead to a higher defect density due to artefact formation.

3.5.2 Lithium decoration

In the past, lithium has been successfully used to decorate defects in silicon wafers. De Kock et al. [93] have used lithium successfully to decorate defects, albeit in single crystal silicon produced by the float zone and pedestal pulling methods. Its behaviour in SOI however, is relatively unknown.

Lithium has a high affinity for oxygen and the oxygen-rich BOX could act as a barrier for its diffusion to the SOI layer. Decoration experiments were therefore conducted not only on standard SOI samples with film and BOX thicknesses of 89 nm and 145 nm respectively but also on a novel SOI material called Extra Thin SOI/Ultra Thin BOX SOI (ETSOI/UTBOX SOI) in which the SOI layer is 20 nm and the BOX just 10 nm thick.

$LiNO_3$ solutions in the concentration range from 0.0001-100 ppm were used for the decoration and, to prevent copper cross contamination in the furnace, a further quartz tube was introduced and used for lithium decoration only. Precautions were taken as outlined in section 3.1 for minimization of cross contamination. After lithium decoration the standard SOI fragments were etched with a dilute Secco (0.04 M Cr (VI)) from their initial SOI layer thickness down to approx. 30-45 nm and ETSOI/UTBOX SOI fragments were etched down to 10 nm with an even more dilute Secco (0.02 M Cr (VI)) due to the very thin SOI films. The samples were then dipped in HF for approx. 90 s (standard SOI) and for approx. 45 s (ETSOI/UTBOX SOI). Selected defects were analyzed in a SEM and AFM.

Further experiments were performed on standard SOI and ETSOI/UTBOX SOI to study the lithium diffusivity throughout the SOI layer. For these studies untreated reference samples were compared to decorated but not etched samples. For lithium decoration $LiNO_3$ solutions in the concentrations 0.0001 and 10 ppm and annealing temperatures of 800, 900 and 950 °C were used for both standard SOI and ETSOI/UTBOX SOI. Separate fragments of standard SOI were also decorated with copper under the same conditions. Secondary ion mass spectrometry (SIMS) measurements were performed to analyze the lithium and copper distribution in the SOI samples after metal diffusion. Hence, these samples were not etched.

On the whole, lithium decoration of SOI samples did not produce satisfactory results. Further experiments are needed to see if lithium is a suitable metal for the decoration of defects in SOI films. However, this is beyond the scope of this study and discussions in the following sections will be confined to the distribution of lithium and copper over a vertical cross-section of the wafer (silicon bulk/BOX/SOI) as determined by SIMS measurements.

3.5.2.1 Standard SOI

All SOI wafer fragments used in the following studies were standard SOI with an 89 nm thick SOI film and a BOX layer of 149 nm. Fig. 3.6 shows a SIMS diagram of an undecorated and unetched standard SOI film. The concentration of both lithium and copper are insignificant.

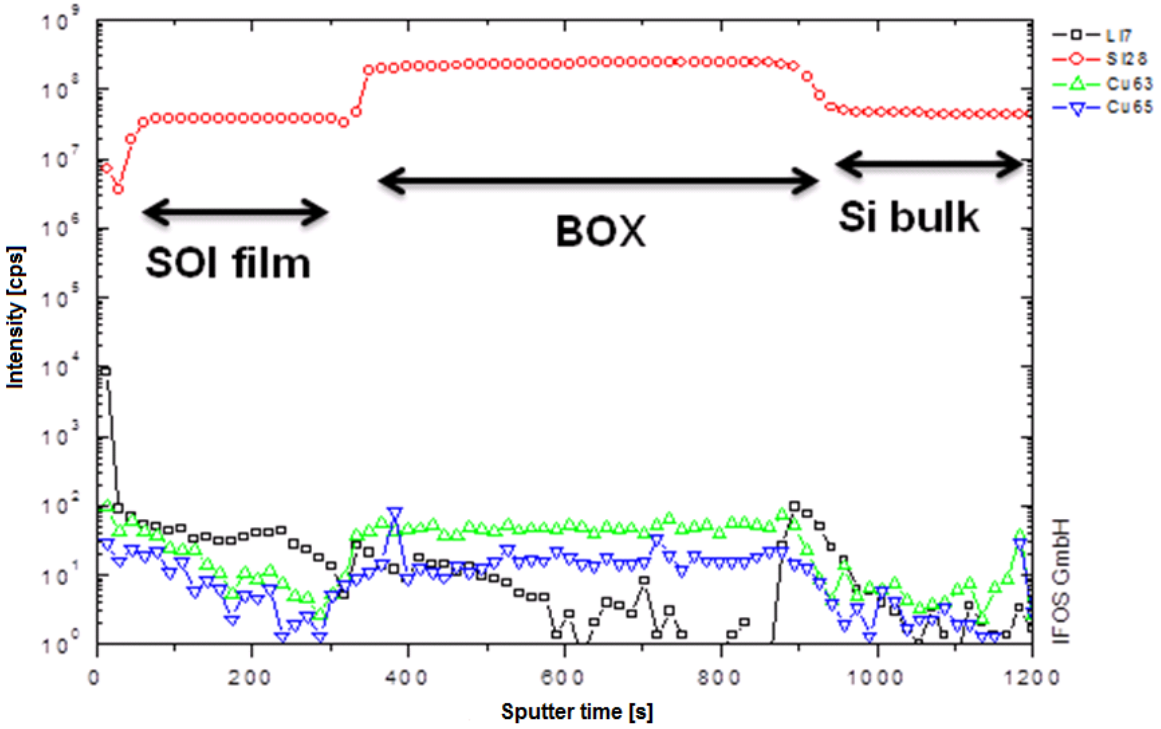


Fig. 3.6 SIMS of a SOI wafer fragment with an 89 nm SOI film and 145 nm BOX, untreated (without decoration and etching).

Fig. 3.7 shows a SIMS profile of a SOI sample decorated with 1 ppm copper, annealed at 800 °C but unetched. Copper easily diffuses through the substrate until it reaches the BOX which is a soft barrier. Then it continues at a lower speed and ends finally in the SOI film where decoration of the defects occurs. Even though the sample was decorated solely with copper lithium could clearly be identified in the SIMS profile. Very likely this has been caused by cross contamination as the same furnace was also used for lithium decoration experiments.

It can clearly be seen that lithium also diffused through the substrate until it reached the BOX. At the BOX/substrate interface the accumulation increases to a maximum indicating that this interface acts as more efficient sink for lithium than the BOX/SOI interface. Moreover, this effect is much more pronounced for lithium than for copper. From the lithium concentration profile we conclude that at the BOX/substrate interface the waferbonding process took place. The high peak of lithium accumulation found at the front side of the SOI film in this SIMS profile may be explained by a gas phase transport of lithium present in the furnace. Lithium also diffuses into the SOI film through the front side reaching the SOI film/BOX interface which again forms a sink and barrier for further diffusion of lithium. Thus both peaks the higher and the lower one find their explanation. It becomes obvious that in copper decoration the copper makes its way through the substrate as expected reaching the SOI film for defect decoration without the BOX forming a strong diffusion barrier. The lithium decoration is mainly the result of a gas phase transport as the BOX contains a large amount of oxygen for which lithium has a high affinity resulting in a higher solubility of lithium in the BOX than in the single crystal silicon of the SOI film and the substrate. It is also obvious that a BOX of 145 nm layer thickness is a too high obstacle for lithium diffusion.

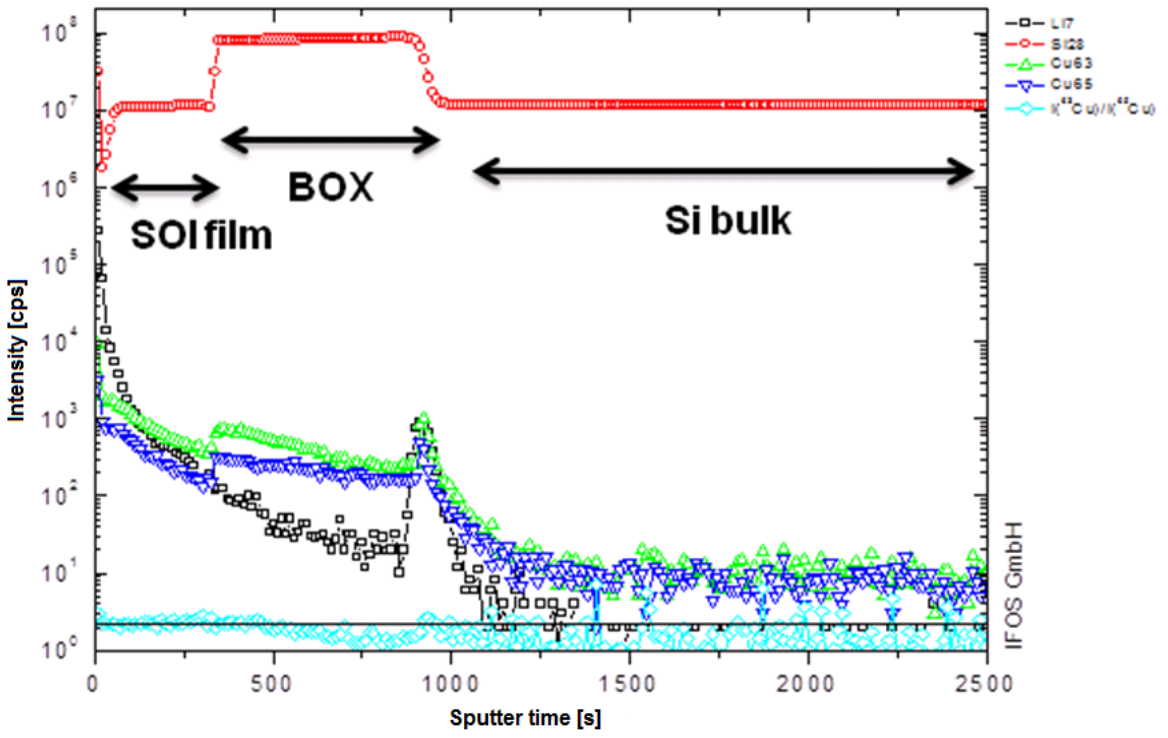


Fig. 3.7 SIMS of a SOI wafer fragment with an 89 nm SOI film and 145 nm BOX, treated with 1 ppm Cu, annealed at 800 °C, unetched.

A SIMS profile of an unetched SOI sample which was decorated with 1 ppm lithium and annealed at 800 °C is shown in Fig. 3.8. Only a small amount of lithium diffused through the

substrate until it reached the BOX. At the BOX/substrate interface again an accumulation of lithium could be observed. The lithium that had diffused through the BOX also passed through the SOI film. Again a high peak of lithium accumulation was found at the front side of the SOI film caused probably by a gas phase transport of lithium in the furnace. Lithium also diffuses through the front side of the SOI film reaching the SOI film/BOX interface and diffusing further into the substrate. Copper is also seen in the spectrum. Its presence may be due to cross contamination as the same furnace had been used previously for copper decoration.

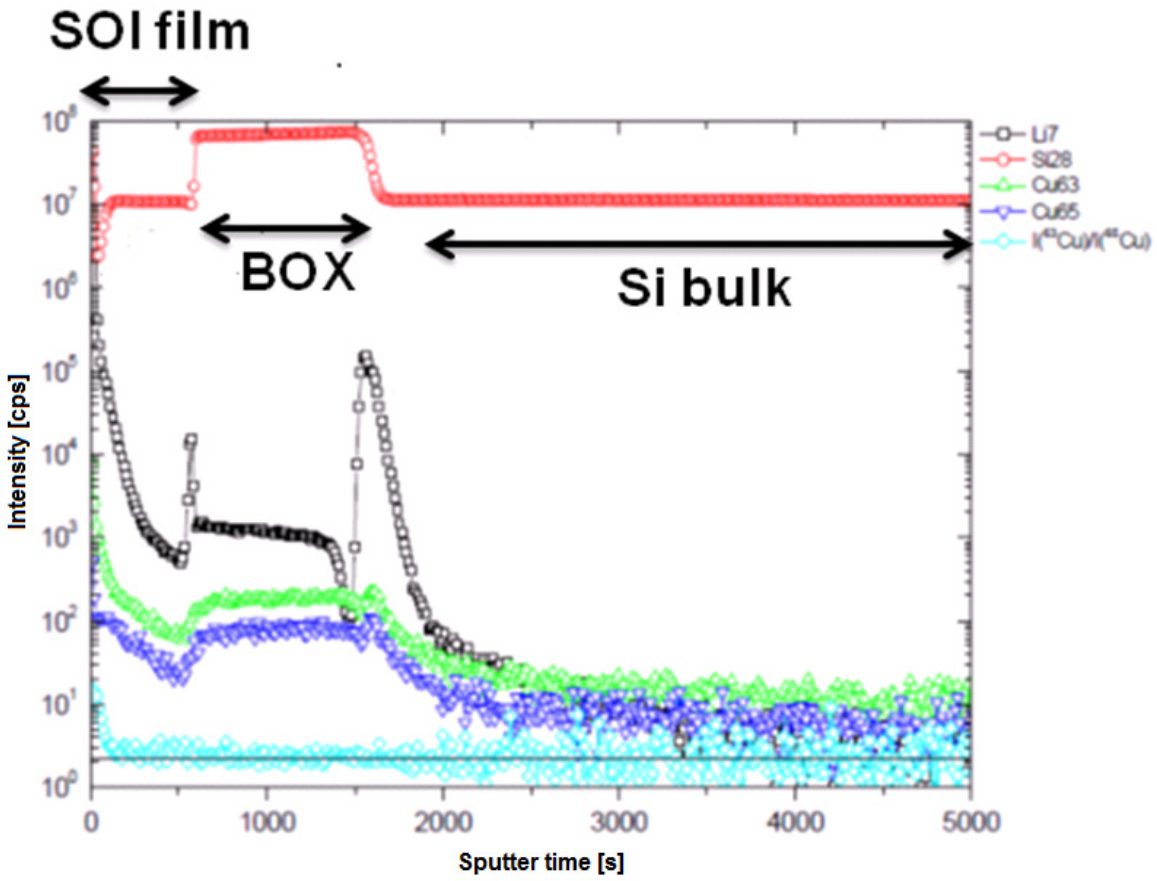


Fig. 3.8 SIMS of a SOI wafer fragment with an 89 nm SOI film and 145 nm BOX, treated with 1 ppm Li, annealed at 800 °C, unetched.

Fig. 3.9 shows an unetched SOI sample which was decorated with 10 ppm of lithium and annealed at 900 °C. An increase in both lithium concentration and annealing temperature led to greater lithium diffusion through the BOX reaching the SOI film. The same happened at the front side of the SOI film via gas phase transport of lithium. Hence, increasing the amount of lithium and the annealing temperature led to diffusion from both front and back surfaces.

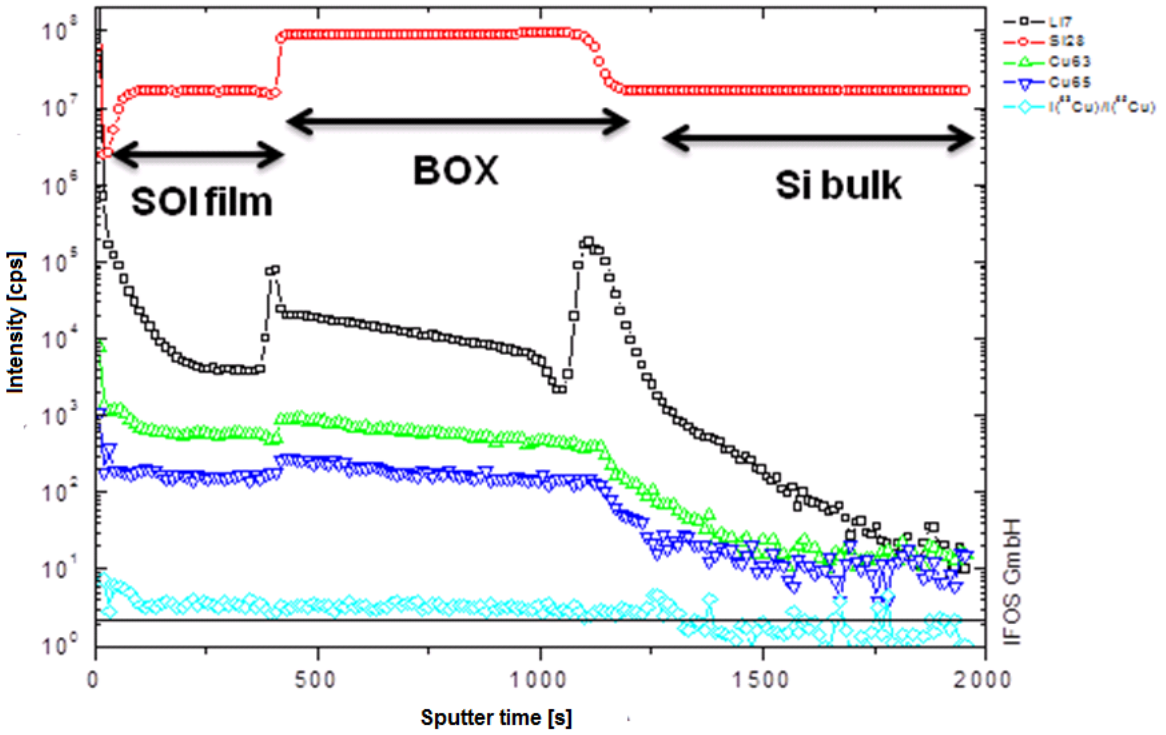


Fig. 3.9 SIMS of a SOI wafer fragment with an 89 nm SOI film and 145 nm BOX, 10 ppm Li, 900 °C, unetched.

Fig. 3.10 gives an overview of some SOI samples analysed. The best lithium diffusion was obtained at an annealing temperature of 900 or 950 °C. The same concentrations of lithium in combination with an annealing temperature of 800 °C led to much less lithium diffusion, since the diffusion coefficient of the diffusing metal grows exponentially with the increase of the annealing temperature. The conclusion which can be drawn is that within limits an increase in lithium concentration only results in improved diffusion in conjunction with an increase in annealing temperature. In the experiments conducted the combination of concentration and temperature which produced the best results was 10 ppm lithium and 900 °C.

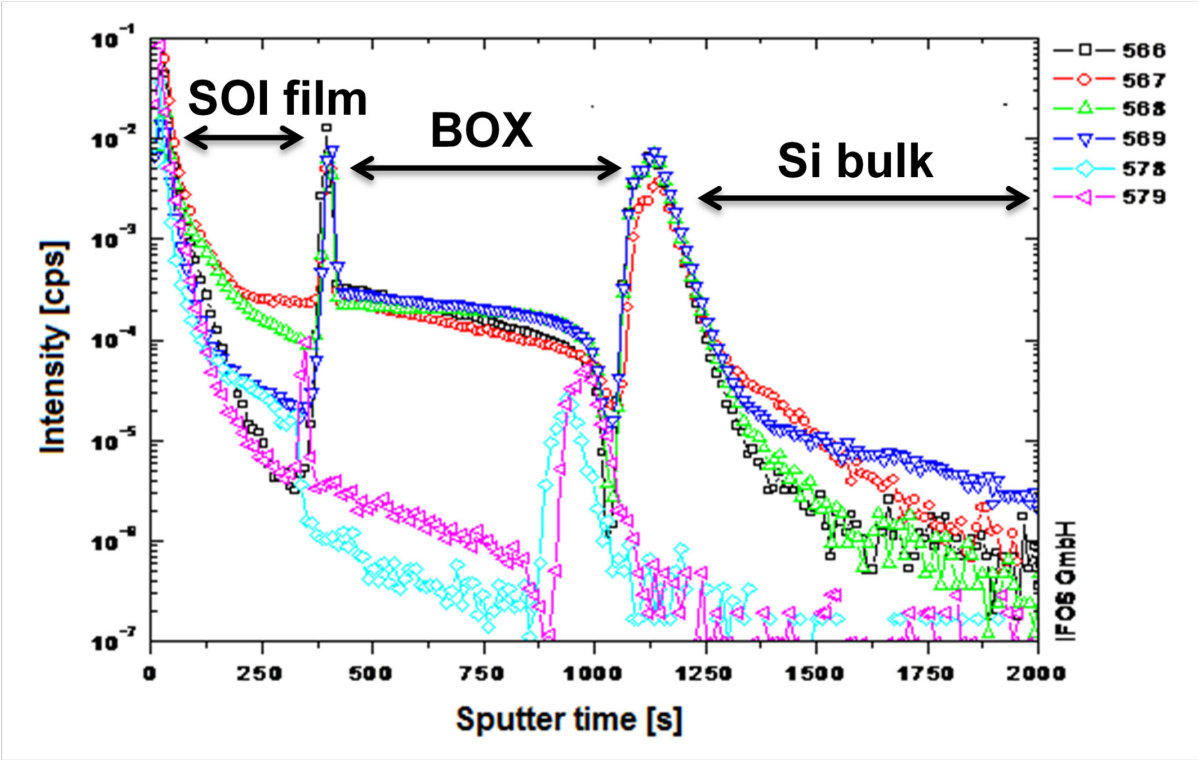


Fig. 3.10 SIMS overview of the following SOI wafer fragments with an 89 nm SOI film and 145 nm BOX, normalized to silicon: 566: 1 ppm Li 900 °C, 567: 10 ppm Li 900 °C, 568: 1 ppm Li 950 °C, 569: 10 ppm Li 950 °C, 578: 1 ppm Li 800 °C, 579: 10 ppm Li 800 °C.

3.5.2.2 ETSOI / UTBOX

All Extra Thin SOI/Ultra Thin BOX SOI (ETSOI/UTBOXSOI) [98] used in the following studies had a SOI film thickness of 20 nm and a BOX layer of 10 nm.

Fig. 3.11 shows a SIMS diagram of an undecorated and unetched wafer fragment of an ETSOI/UTBOXSOI. Both lithium and copper could be detected in low concentrations as a result of cross contamination.

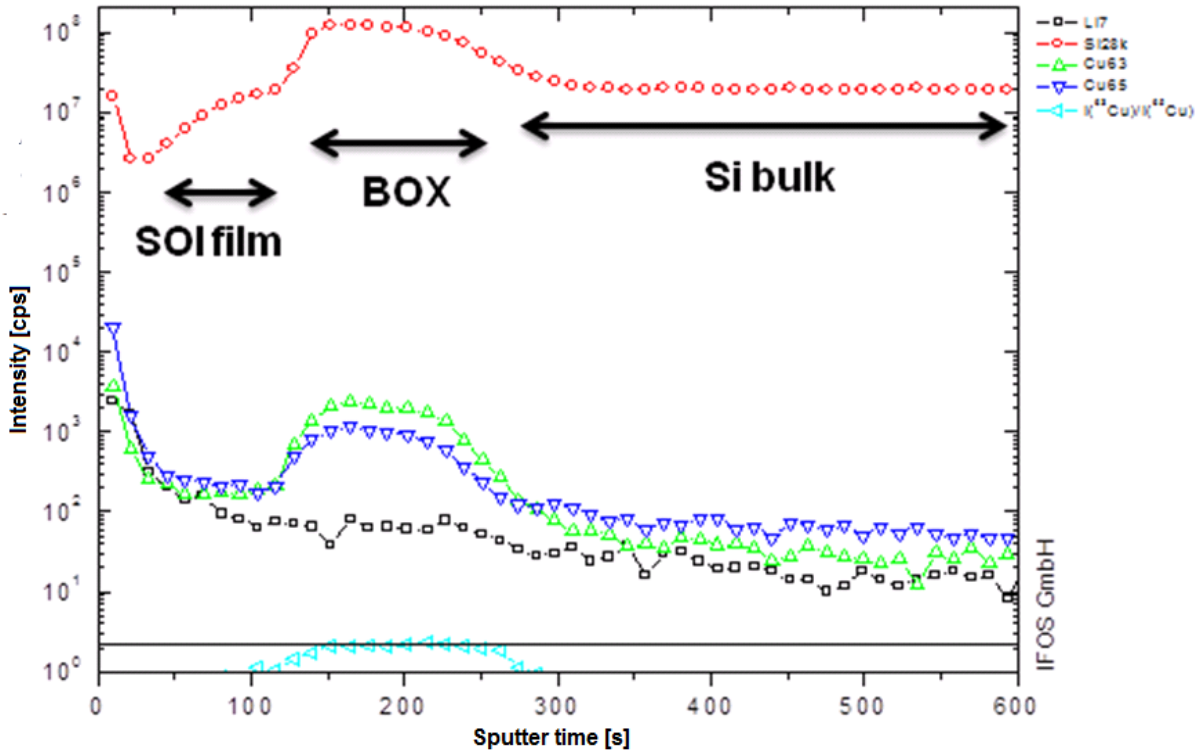


Fig. 3.11 SIMS of an ETSOI/UTBOX SOI wafer fragment with a 20 nm SOI film and 10 nm BOX, untreated (without decoration and etching).

Fig. 3.12 shows an ETSOI/UTBOX decorated with 10 ppm of lithium at an annealing temperature of 900 °C. It can clearly be seen that enough lithium diffuses though the substrate reaching the BOX as a lower barrier in order to push through to the SOI film. The ultrathin BOX forms a considerably lower obstacle than the 145 nm standard BOX. And again, lithium diffusion occurs through the front surface of the wafer fragment as a result of a gas phase transport.

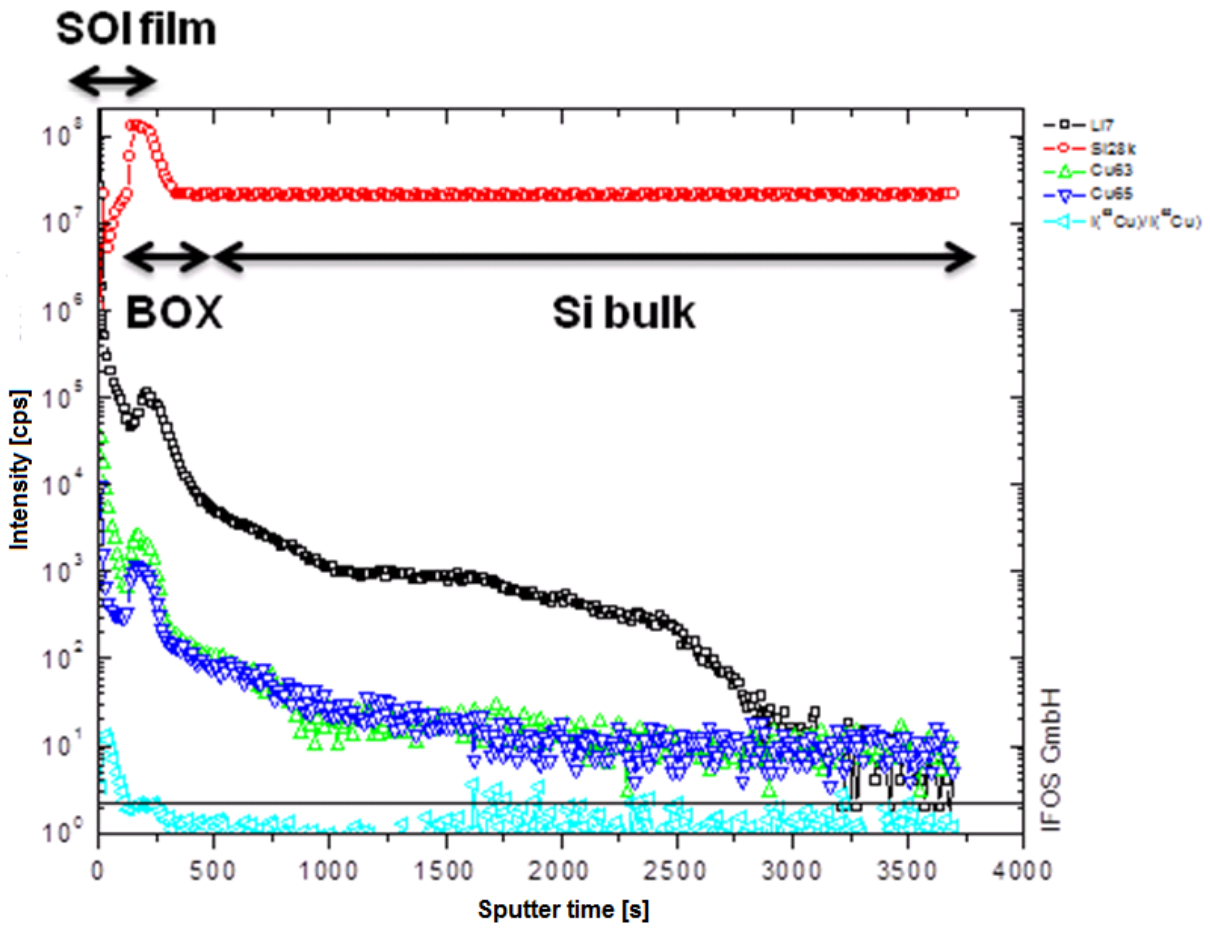


Fig. 3.12 SIMS of an ETSOI/UTBOX SOI wafer fragment with a 20 nm SOI film and 10 nm BOX, 10 ppm Li, 900 °C, unetched.

Fig. 3.13 gives an overview of some ETSOI/UTBOX SOI samples analysed via SIMS. An annealing temperature of 900 °C seems to be the better option for lithium diffusion to the SOI film. The small difference in intensity between 0.0001 ppm lithium and 10 ppm lithium at 900 °C indicates that the optimum concentration for lithium decoration could lie somewhere in between. At 10 ppm, the relatively larger amount of lithium that either remains in the substrate and BOX or has diffused from the front through the SOI film suggests that a smaller concentration would suffice.

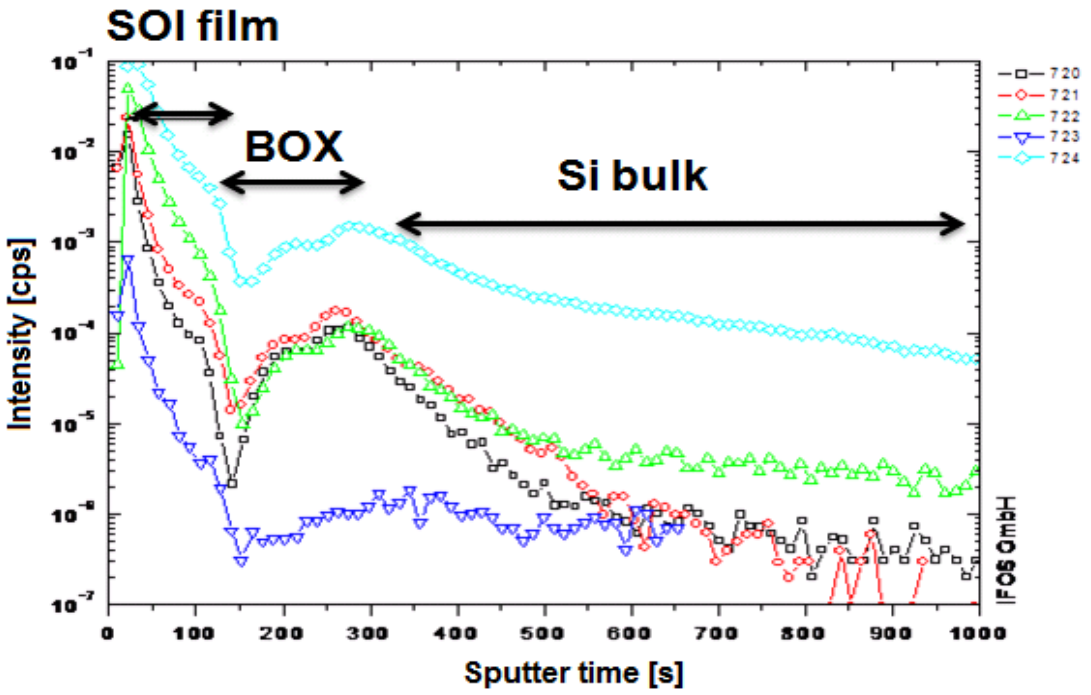


Fig. 3.13 SIMS overview of of an ETSOI/UTBOX SOI wafer fragment with a 20 nm SOI film and 10 nm BOX, normalized to silicon: 720: 0.0001 ppm Li 800 °C, 721: 10 ppm Li 800 °C, 722: 0.0001 ppm Li 900 °C, 723: Reference (untreated), 724: 10 ppm Li 900 °C.

Conclusion

Before the decoration of defects with lithium can be considered, several factors have to be taken into account. Copper decoration of SOI wafers requires diffusion through the back of the wafer as copper tends to precipitate on the surface forming artefacts, which would be a hindrance to defect detection if applied directly on the SOI surface. With lithium, on the other hand, the BOX layer acts as a barrier to diffusion and a 145 nm BOX layer is definitely too thick. Where the BOX layer is thin, as in ETSOI/UTBOXSOI, lithium diffuses through without much hindrance and may be better suited than copper as it hardly forms artefacts. For standard and thick SOI, further studies will have to be undertaken to find the best combination of concentration and annealing temperature and to see if diffusion from the gas phase onto the SOI surface is a viable alternative.

3.6 Electrochemical copper deposition out of a dilute $Cu(NO_3)_2$ spiked hydrofluoric acid solution

Copper decoration via furnace annealing is a well established method to delineate crystal defects which are so small as to escape detection with conventional methods of delineation. The drawback of this procedure is the tendency to form artefacts through copper cross contamination in the furnace. To avoid the formation of artefacts an attempt was made to deposit copper electrochemically out of a diluted $Cu(NO_3)_2$ spiked hydrofluoric acid solution on the SOI film surface [99-107]. By this "wet-chemical" copper deposition it should be possible to bypass this problem since this electrochemical procedure does not include any annealing step. Electrochemical copper deposition leads to the nucleation and growth of metallic copper particles on the surface [99, 101] which may nucleate preferentially at surface defect sites.

The experiments were performed on standard SOI with an initial layer thickness of about 90 nm and on sSOI with initial layer thicknesses of about 14 and 64 nm. The BOX layer thickness for both materials was about 145 nm. Some of the fragments received just an electrochemical copper deposition treatment; others after electrochemical copper deposition were subsequently etched with a dilute Secco (0.04 M Cr (VI)) etch. Some of the sSOI fragments were etched with OPE D [108].

For the decoration procedure the SOI fragments were placed vertically in a Teflon™ sample-holder and dipped for 1 min in a 5% hydrofluoric acid solution containing 0.01-10 ppm (SOI) and 0.01-1 ppm (sSOI) of $Cu(NO_3)_2$. The solution was not stirred. The samples were then rinsed in Millipore water for two minutes and dried with short blasts of nitrogen.

This procedure could cause metallic copper particles to nucleate preferentially at surface sites of increased surface potential such as surface and crystal defects.

SOI etched with dil. Secco

The light optical micrograph of Fig. 3.14 (left) shows a standard SOI fragment which was decorated via electrochemical copper deposition displaying a high density (3×10^5 cm^{-2}) of randomly distributed red particles.

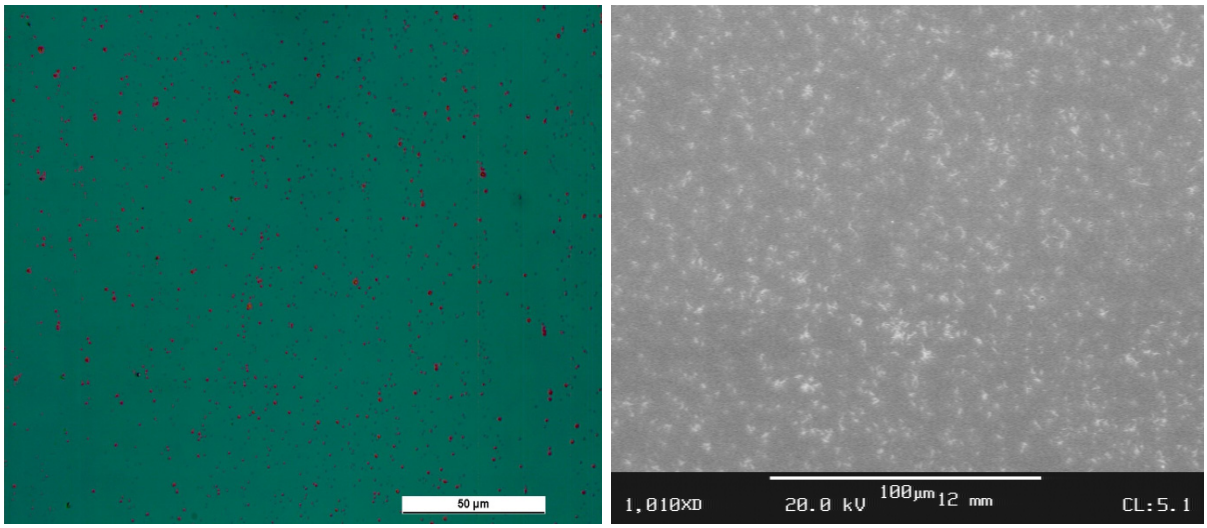


Fig. 3.14 SOI sample after electrochemical copper decoration with 1 ppm Cu in 5% HF solution for 1 min; without etching. Left: light optical micrograph, high density of copper particles on the surface; right: in the secondary electron SEM image of the same sample.

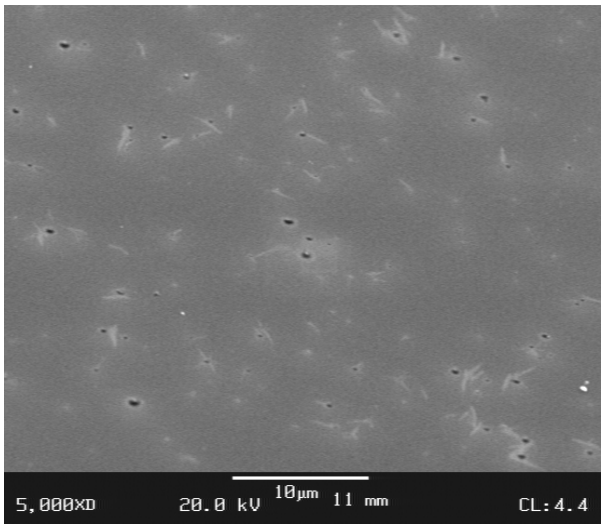


Fig. 3.15 Fivefold magnified image of the sample in Fig. 3.14.

Fig. 3.14 (right) and Fig. 3.15 show secondary electron SEM images of the same sample. The defects appear as bright points corresponding to increased secondary electron emission attributable to metallic copper particles. Although copper could not be detected by SEM/EDX, in similar experiments conducted by G. Glanz [109] clear evidence for metallic copper on the surface was obtained using the more surface sensitive X-ray photoelectron spectrometer. In addition some dark dot-like contrasts are displayed. These correspond to pits in the SOI film produced by a corrosive interaction between some copper particles and the silicon [99].

Another SOI fragment was decorated with copper under the same conditions and then etched with a dilute Secco etching solution (0.04 M Cr (VI)) followed by a dip in hydrofluoric acid to reveal the defects (Fig. 3.16).

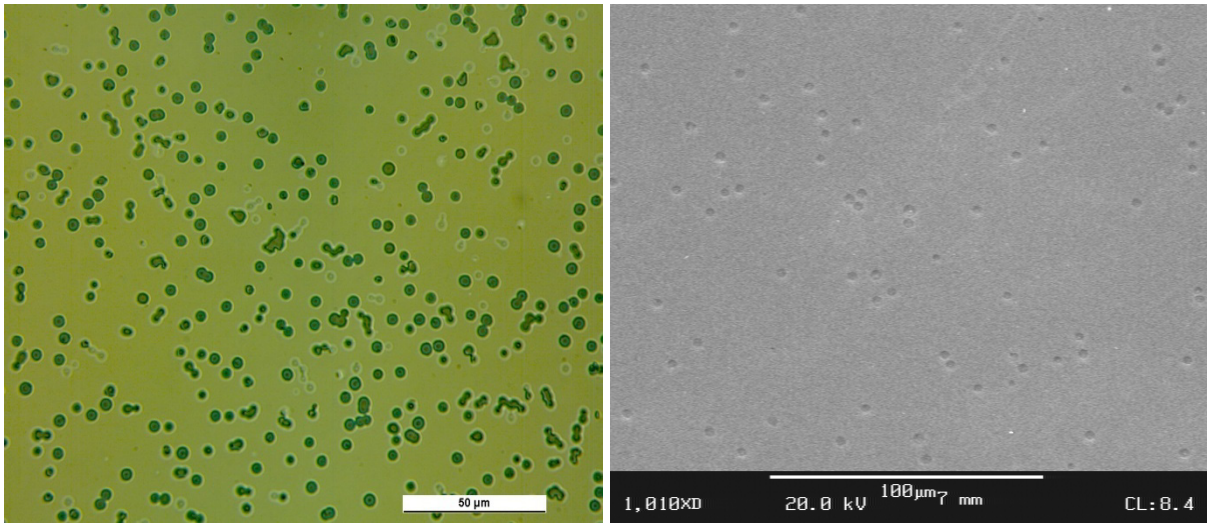


Fig. 3.16 SOI Sample after electrochemical copper decoration with1 ppm Cu in 5% HF solution for 1 min, followed by etching with dilute Secco (0.04 M Cr (VI)) and a dip in HF for 90 s. The light optical micrograph (left) displays a high defect density of approx. 300 000 cm^2; right: SEM image of the sample.

The light optical micrograph in Fig. 3.16 displays a defect density of approx. 3 x 10^5 cm^{-2} which is much higher than the typical defect densities of SOI fragments decorated with the same copper concentration via furnace annealing (DD: approx. 2.2 x 10^4 cm^{-2}, see section 3.7.1).

The reason for this very high density is random nucleation of metallic copper particles on the sample surface which in the subsequent Secco etching results in enhanced etching of the silicon at the copper particle site producing a channel down to the BOX. In the dip in HF that follows the underlying BOX is etched in the usual manner as illustrated by the SEM images of this sample in Fig. 3.16 and Fig. 3.17 at different magnifications.

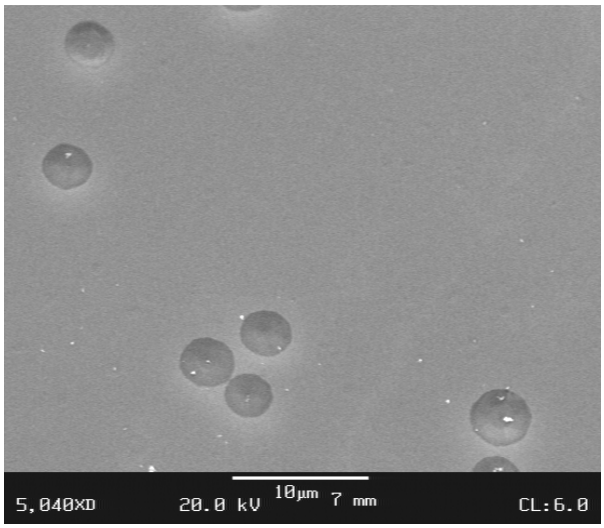


Fig. 3.17 Fivefold magnification of right hand image in Fig. 3.16.

Conclusion

The results obtained of this type of decoration experiments lead to the conclusion that on SOI wafers the electrochemical copper deposition out of a $Cu(NO_3)_2$ spiked hydrofluoric acid solution is unsuitable for reliable delineation of crystal defects such as COPs which do not produce any significant strain field in the surrounding silicon lattice.

sSOI etched with dil. Secco

Electrochemical copper deposition studies were also performed on 14 and 64 nm thick sSOI materials and the conditions for decoration were optimized.

14 nm sSOI

All the samples were generally etched with a dilute Secco 0.04 M (Cr (VI)) for 12 s and subsequently dipped in HF for 8 s to etch the underlying BOX.

The light optical micrograph of Fig. 3.18 shows a reference 14 nm sSOI fragment (Ref 1). A high density of point-like etch features appointed to threading dislocations (TD) and some linear arrays of dots associated with stacking faults (SF) are visible.

Fig. 3.18 Light optical micrograph of a reference 14 nm sSOI fragment (Ref 1), residual layer thickness: 8 nm. Some SF and a high density of TD are visible. Magnification: 1 000x.

Fig. 3.19 shows a light optical micrograph (left) and a SEM image (right) of a 14 nm sSOI which was decorated with 0.1 ppm copper via electrochemical copper deposition. SFs and TD are clearly visible as lines and pits respectively.

The SEM image in Fig. 3.20 shows a magnified view of the same sSOI sample as in Fig. 3.19. Both SEM images show dots which may correspond to TDs and arrays of lines and dots which can be ascribed to SF.

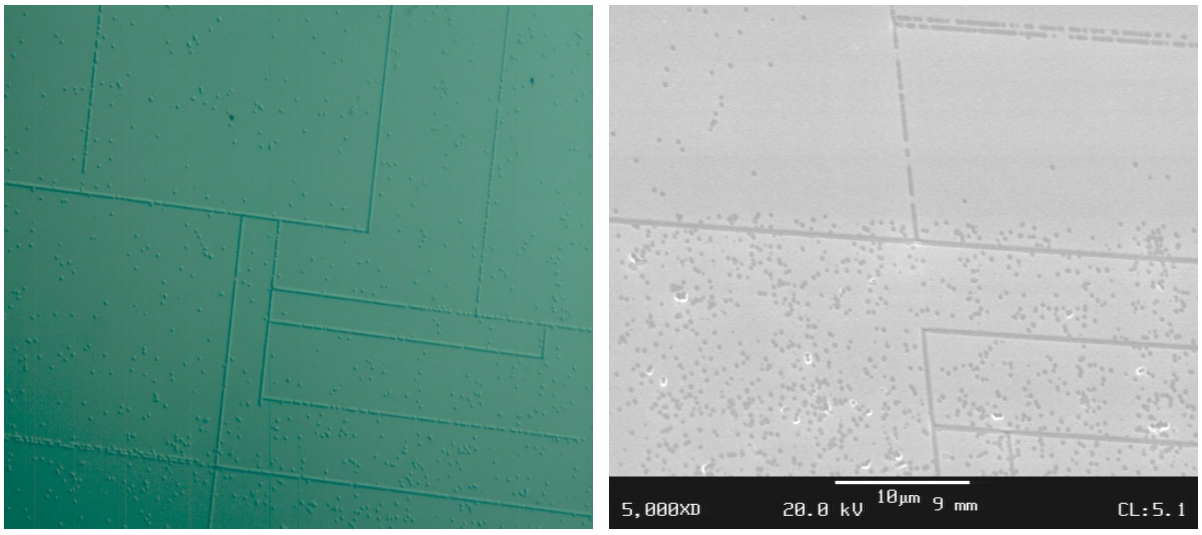


Fig. 3.19 Light optical micrograph (left, magnification: 1 000x) and a SEM image (right, magnification: 5 000x) of a 14 nm sSOI fragment decorated with 0.1 ppm copper via wet-chemical copper deposition. Residual layer thickness: 8.5 nm. Dots may be ascribed to TDs and arrays of lines and dots to SF.

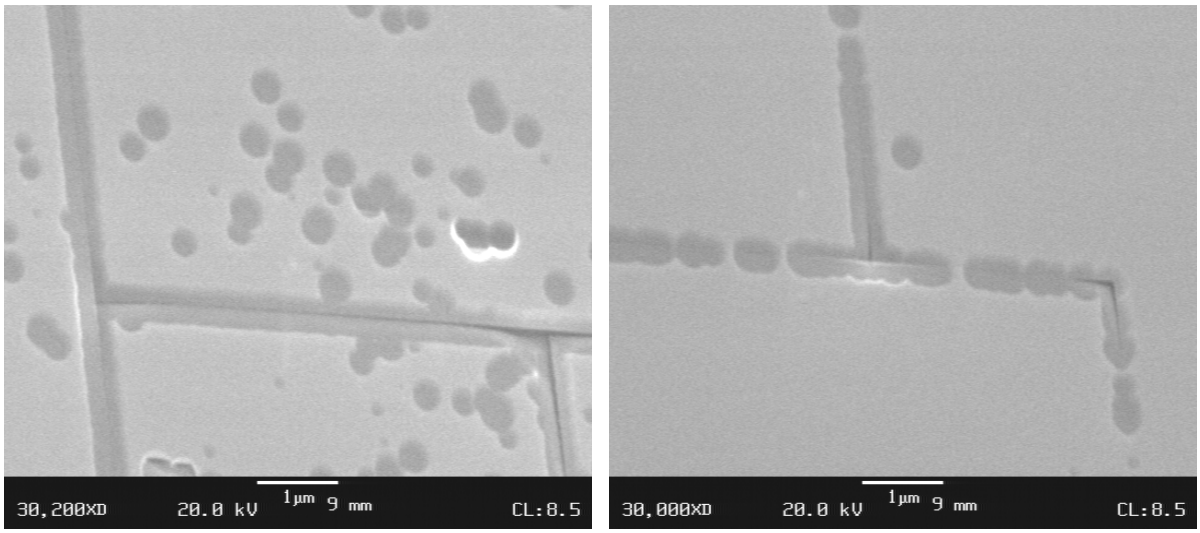


Fig. 3.20 SEM images of a 14 nm sSOI fragment (same sample as in Fig. 3.19) decorated with 0.1 ppm of copper via wet-chemical copper deposition. Residual layer thickness: 8.5 nm. Dots may be ascribed to TDs and arrays of lines and dots to SF. Magnification: 30 000x.

Another 14 nm sSOI fragment was decorated with 1 ppm copper under the same conditions and subsequently etched with a dilute Secco (Fig. 3.21). The higher copper concentration and the associated increase of the etch rate and artefact formation caused a partial delamination of the thin sSOI film.

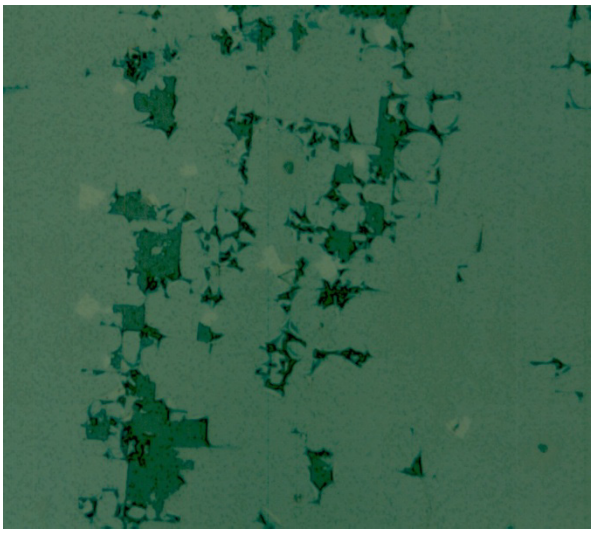


Fig. 3.21 Light optical micrograph of a 14 nm sSOI fragment decorated with 1 ppm of copper via wet chemical copper deposition and etched with dil. Secco for 9 s. Residual layer thickness: 7.0 nm. Magnification: 1 000x.

Conclusion

The best results obtained with electrochemical copper deposition were with a 0.1 ppm copper spiked solution which revealed both TD and SF in thin sSOI (14 nm) without delamination of the sSOI film.

64 nm sSOI

All the samples were etched with a dilute Secco (0.04 M (Cr (VI)) for either 30 s or 47 s and then dipped in HF for 8 s to reveal the defects.

Fig. 3.22 shows a light optical micrograph of a reference sSOI fragment (Ref 1) which was etched for 30 s. A few threading dislocations (TD) and stacking faults (SF) are visible. A residual layer thickness of more than 50% of the initial layer appears to be the reason for the comparatively low defect density.

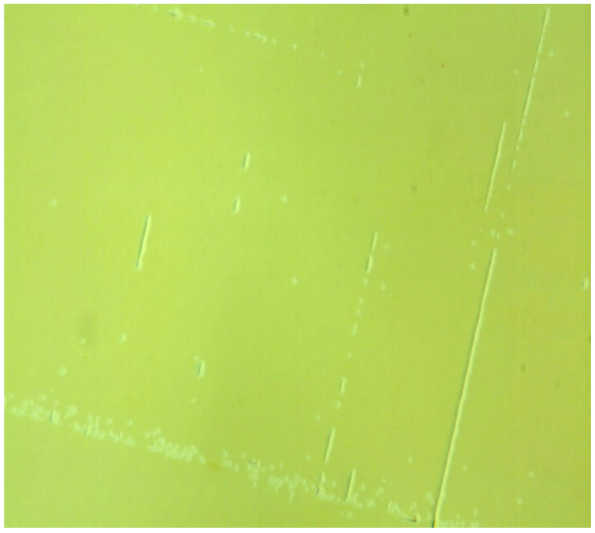


Fig. 3.22 Light optical micrograph of a reference 64 nm sSOI fragment (Ref 1) etched with dil. Secco for 30 s. Residual layer thickness: 39.6 nm. A few TD and SF are visible. Magnification: 1 000x.

Both Fig. 3.23 and Fig. 3.24 display light optical micrographs of sSOI fragments which were decorated with 1 ppm copper under the same conditions. They only differ in their etching times and, hence, their residual layer thicknesses:

- The sample shown in Fig. 3.23 was etched for 30 s resulting in a residual layer thickness of 42.1 nm. A few threading dislocations (TD) and stacking faults (SF) are visible.

- The sample shown in Fig. 3.24 was etched for 47 s resulting in a residual layer thickness of 28.9 nm. A very high DD of SFs and some delamination in patches of the sSOI layer can be seen.

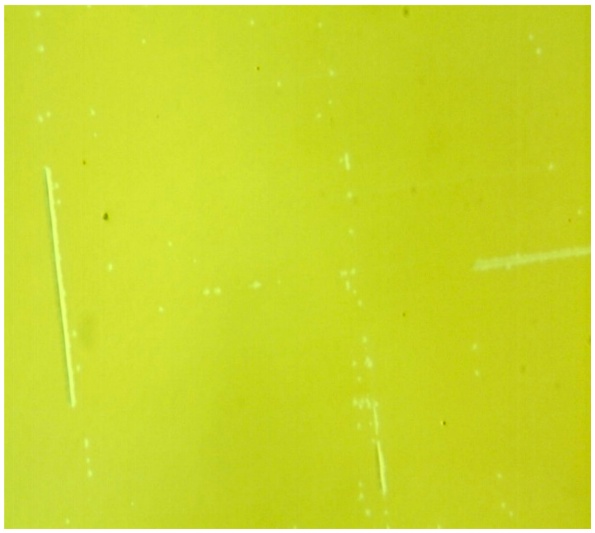


Fig. 3.23 Light optical micrograph of a 64 nm sSOI fragment electrochemically decorated with 1 ppm of copper and etched with dil. Secco for 30 s. Residual layer thickness: 42.1 nm. A few TD and SF are visible. Magnification: 1 000x.

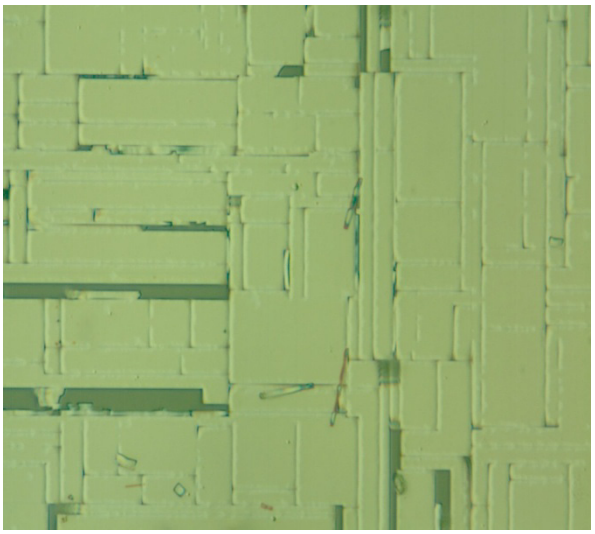


Fig. 3.24 Light optical micrograph of a 64 nm sSOI fragment electrochemically decorated with 1 ppm of copper and etched with dil. Secco for 47 s. Residual layer thickness: 28.9 nm. A few TD and and a comparatively high density of SF are visible. Partial delamination of the sSOI layer. Magnification: 1 000x.

Conclusion

These results show that sSOI fragments with a strained silicon film of 64 nm should be etched down to less than 50% of the initial sSOI film to reach the defects for their delineation.

sSOI etched with OPE D

Electrochemical copper deposition studies were also conducted on 64 nm sSOI using the chromium-free OPE D as the etching solution for defect delineation. All the samples were etched for 25 min. OPE D has a very slow etch rate, hence the long etching times. This together with the fact that HF is a component of OPE D made the subsequent dip in HF unnecessary.

The light optical micrograph in Fig. 3.25 shows a reference sample (Ref 1). Bright (right magnified view) and dark TDs (left magnified view) are visible. The bright TDs represent defects where most of the sSOI layer around the defects is still present. The dark TDs exhibit defects where the sSOI film has sunk to the base of the pit which in this case is the silicon substrate. Hence, these defects appear dark in the light optical microscope image. Stacking faults were not revealed after etching with OPE D which is apparently unsuitable for their delineation in sSOI (see section 3.10).

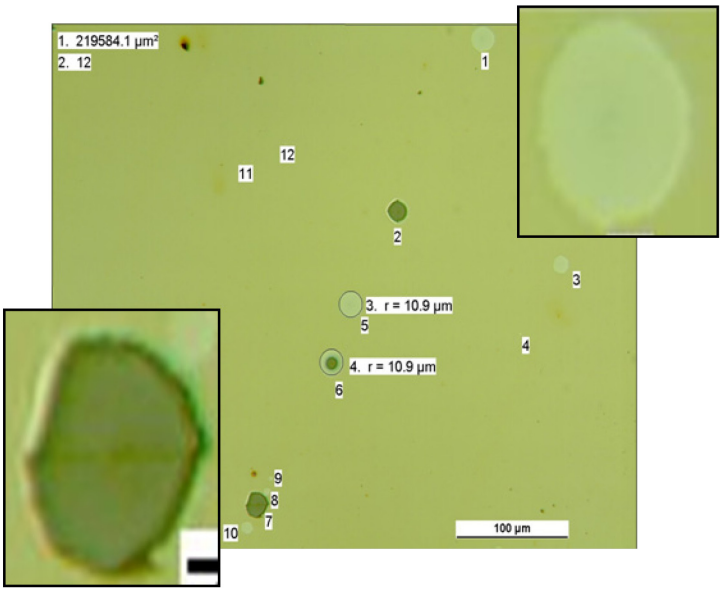


Fig. 3.25 Light optical micrograph of a Ref 1 64 nm sSOI fragment. Residual layer thickness: 39 nm. Only TD are visible. Inserts: magnified view.

Fig. 3.26 shows light optical micrographs of two sSOI fragments which were decorated with 0.1 ppm (left) and 1 ppm (right) copper via electrochemical copper deposition and subsequently etched with OPE D. Decoration with 0.1 ppm of copper resulted in bright TDs

with an intact sSOI layer at the defect and dark TDs with a bright halo. The dark spots are defects where the SOI film has sunk to the base of the pit.

With a copper concentration of 1 ppm predominantly dark defects were delineated, some with, and others without a halo. Bright defects were hardly seen. There is just one bright defect in the center of the figure. A few defects were seen with spiral type features in the sunk sSOI film. These could be linked to threading dislocations of dominating screw component (see right magnified view). The radii of the TDs are larger than those of the samples decorated with 0.1 ppm of copper. Stacking faults were not visible even after copper decoration.

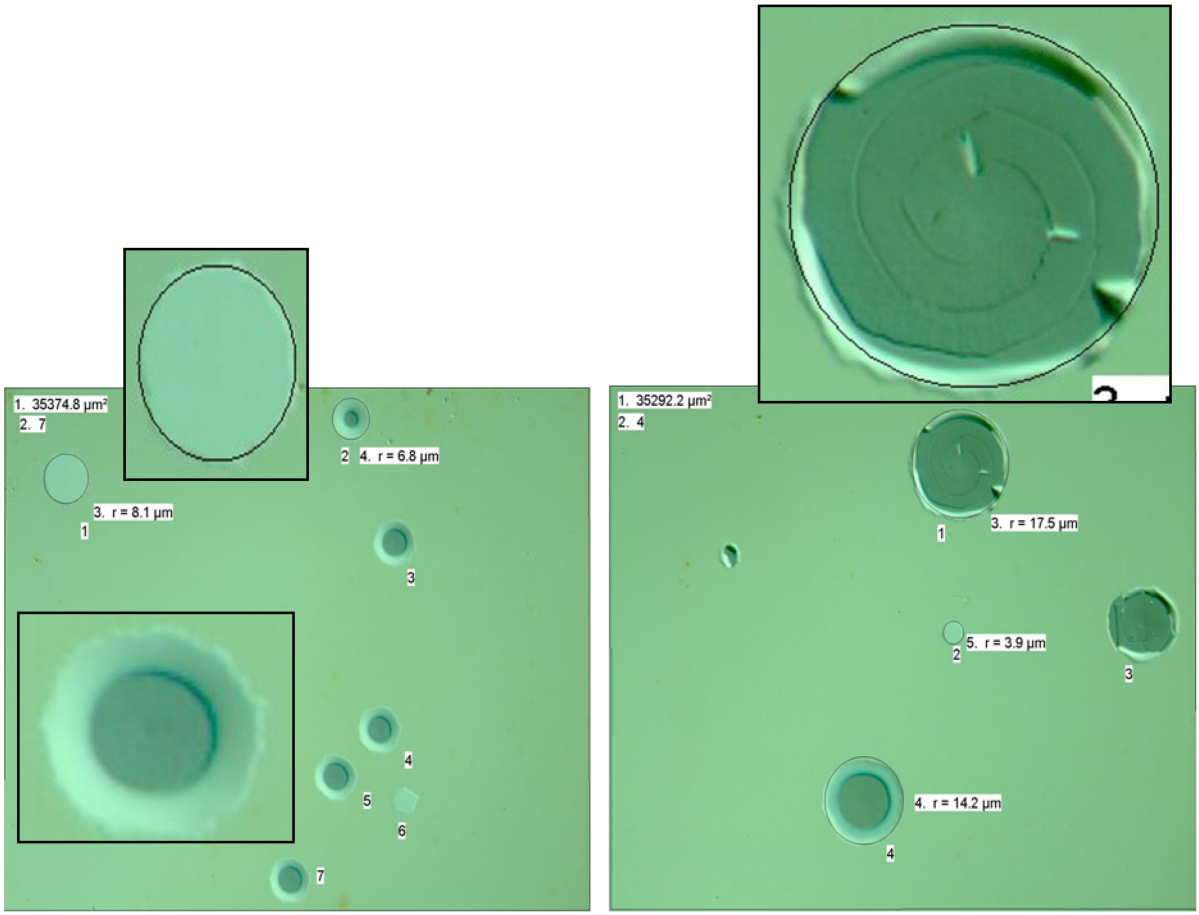


Fig. 3.26 Light optical micrographs of 64 nm sSOI fragments electrochemically decorated with 0.1 ppm (left) and 1 ppm (right)) of copper. Residual layer thickness: 33.1 nm with 0.1 ppm and 33.7 nm with 1 ppm copper. Only TD visible. Magnification: 500x. Inserts magnified view.

For a detailed examination a sample decorated with1 ppm copper was analysed using SEM (Fig. 3.27). The SEM image on the left shows several TDs, some with a spiral pattern which may be linked to “screw dislocation-like defects”. The SOI film of most of the defects had sunk down to the substrate. The SEM image on the right is a magnified view of a defect which appears to be a screw dislocation due to its structure.

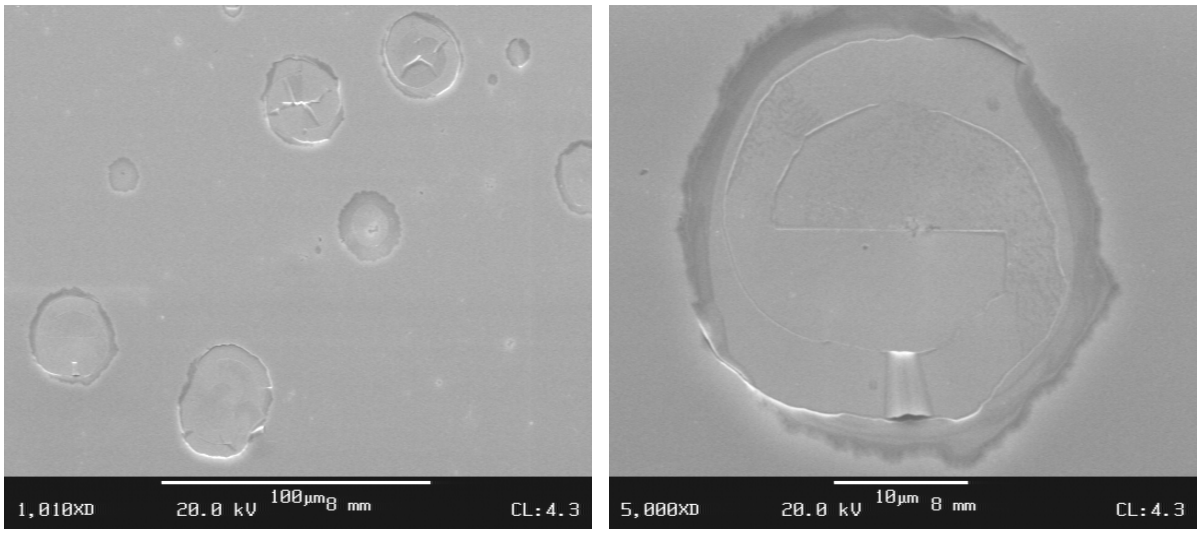


Fig. 3.27 SEM images of a 64 nm sSOI fragment electrochemically decorated with 1 ppm of copper (same sample as in Fig. 3.26). Residual layer thickness: 33.1 nm. TD (left) and a magnified view of a screw dislocation-like defect (right) are visible. Magnification: 1 000x (left), 5 000x (right).

3.7 Copper decoration via furnace annealing of standard SOI

For copper decoration with furnace annealing of standard SOI (SOI layer thickness of about 60-150 nm, BOX layer thickness of 145 nm) the experimental parameters which were largely determined in a previous study [108] were as follows:

- Suitable copper concentration in $Cu(NO_3)_2$ solution is ≤ 1 ppm
- Suitable volume of $Cu(NO_3)_2$ solution to be deposited on the back of the SOI fragment is 0.5 µL
- Annealing temperature: 800 °C

In earlier experiments [110] the optimal temperature for the diffusion of Cu through a BOX of 145 nm to the SOI layer was found to be 800 °C (see SIMS measurements in section 3.5.2). This makes the BOX a low diffusion barrier for copper.

Fig. 3.28 shows a non decorated reference sample with a low defect density (DD: 450 cm^{-2}).

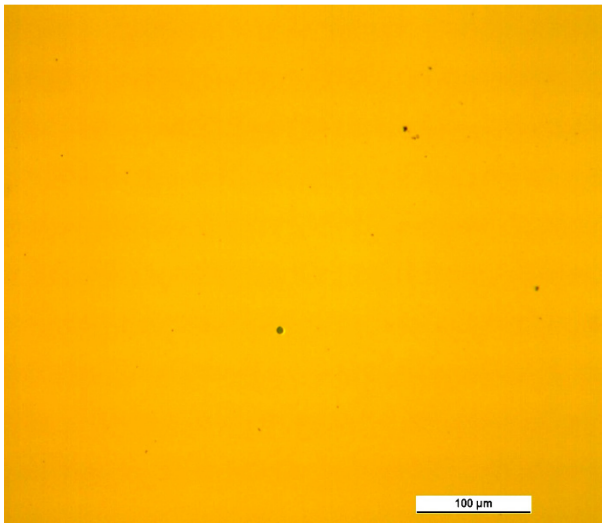


Fig. 3.28 Light optical micrograph of a 90 nm SOI Ref 1 sample, etched with dilute Secco (0.04 M Cr (VI)), dipped in HF for 90 s. DD = 450 cm^{-2}.

A copper decorated sample after etching with dilute Secco solution is shown in Fig. 3.29 (DD: 45 000 cm^{-2}). The defect density is much higher than that of the reference sample.

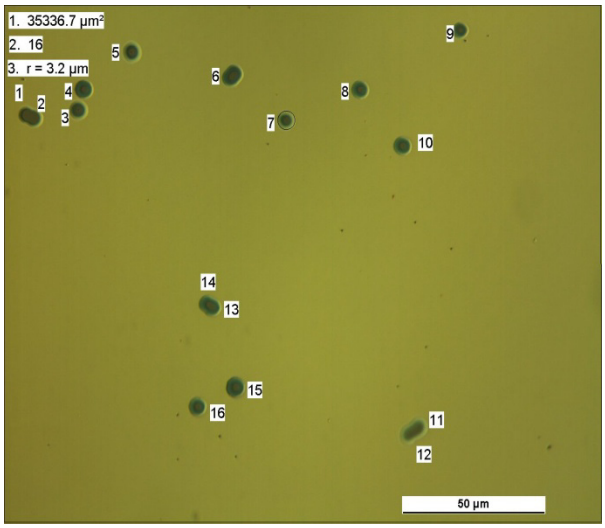


Fig. 3.29 Light optical micrograph of a 90 nm SOI fragment decorated with 1 ppm Cu, annealed for 1 min at 800 °C; etched with dilute Secco (0.04 M Cr (VI)) and dipped in HF for 90 s. DD = 45 000 cm^{-2}.

The higher defect density may be attributed to small defects in the SOI layer decorated by copper. These are not detected by Secco etching in non-decorated samples. However, it may to some extent be ascribed to artefacts induced by copper precipitation. An unexpectedly higher defect density was sometimes also obtained at copper concentrations below 1 ppm. This effect was presumably caused by copper cross contamination in the furnace used.

The main source of artefact formation was the copper cross contamination in the quartz tube in the furnace used. To minimize cross contamination, the fragments were first placed in a quartz tube which was then introduced into the quartz tube of the furnace. The inner quartz tubes were cleaned periodically to remove residual copper. It cannot be ruled out that cross contamination in the furnace contributed to any of the DDs obtained after furnace annealing. However, owing to the precautions taken it can be assumed that this contribution is not substantial.

A further defect type, which appeared as red spots in the light optical micrograph after decoration, had been discovered in copper decorated standard SOI fragments in a previous study [110]. Red spots appeared with varying spatial distribution in most of the SOI fragments from an earlier batch of wafers. The defect density of the red spots was about 2.8 x 10^3–15 x 10^3 cm^{-2} with the diameter of a red spot being approx. 2 µm. Fig. 3.30 shows an example of a copper decorated standard SOI fragment which exhibits a high density of red spots (DD: 147 000 cm^{-2}).

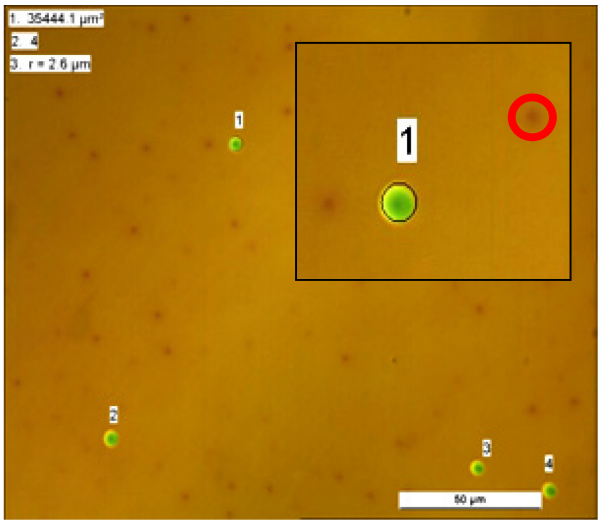


Fig. 3.30 Light optical micrograph of a SOI fragment decorated with 0.001 ppm Cu annealed at 800 °C for 1 min; etched with dilute Secco (0.04 M Cr (VI)), dipped in HF for 90 s. DD: 450 cm^{-2}. DD of red spots: 147 000 cm^{-2}, diameter of a red spot: approx. 2 µm.

The red spots appear in the light optical micrograph as bumps on the surface and are probably caused when copper has settled in one of the two interfaces and/or light absorption effects of the metallic copper silicide precipitates [108]. The silicide Cu_3Si is metallic and therefore absorbs more light.

In model furnace annealing experiments and TEM investigations with silicon substrates covered by thin (20-30 nm) thermally grown SiO_2 that have been intentionally contaminated with copper it has been demonstrated that the copper silicide precipitates formed at the Si/SiO_2 interface during the cooling period cause thinning and/or arching upwards of the thin oxide layer or even protrusion into the oxide layer. The reason is a volume expansion of 230% produced by the formation of copper silicide (Cu_3Si) in the silicon at the Si/SiO_2 interface. The red spots can be explained in a similar manner: these copper decorated defects may be located in one of the two interfaces of a SOI-wafer (Fig. 3.31) viz. the SOI-film/BOX or the BOX/Si substrate.

These Cu-contamination-induced defects in the SOI-film were named “CDF” if they were located at the SOI-film/BOX interface and “CDS” if they were located at the BOX/Si substrate interface.

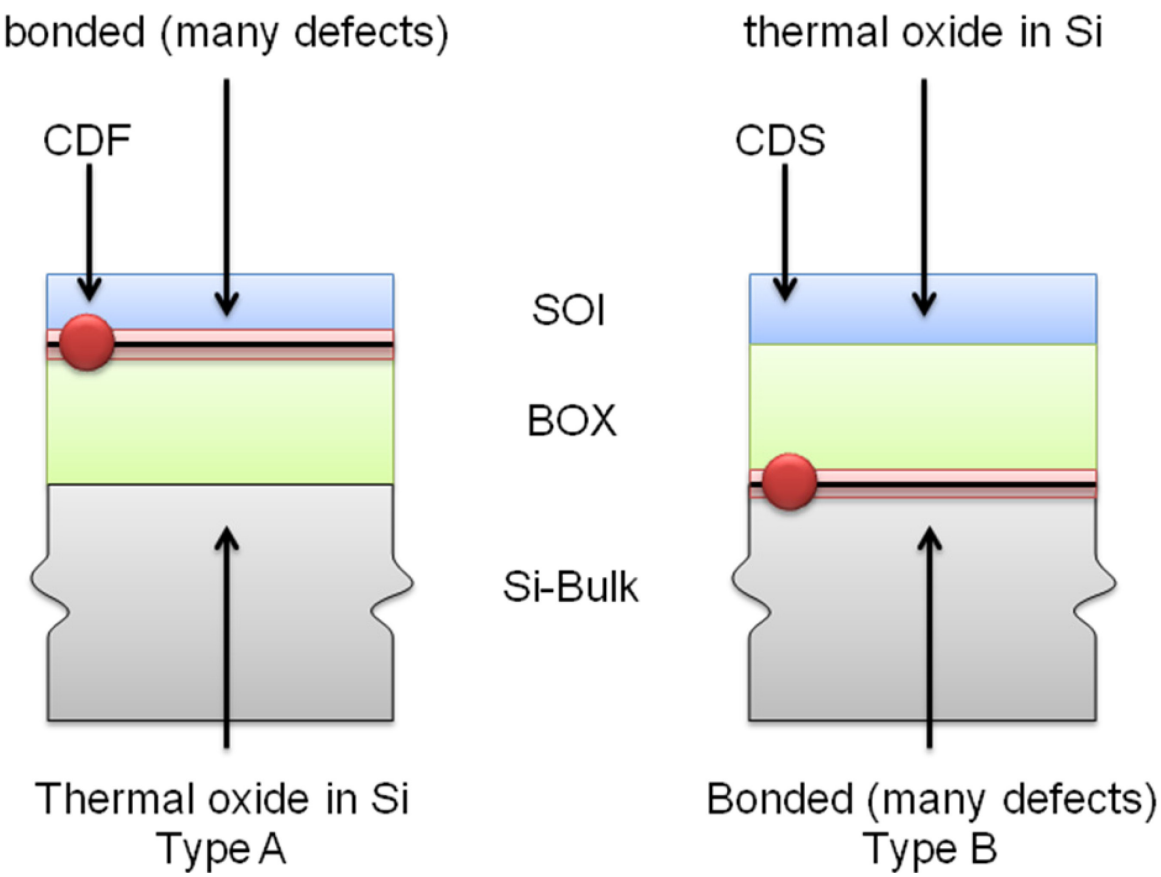


Fig. 3.31 Scheme of a copper decorated SOI-wafer. The red spots may be located in one of the two interfaces of a SOI-wafer: either the SOI-film/BOX or the BOX/Si-substrate; layer thicknesses: approx. 90 nm SOI, 145 nm BOX, and approx. 600-700 µm Si-Bulk.

Fig. 3.31 shows a scheme to illustrate the origin of the red spots. In type A the bonded site in the SOI-wafer is the interface SOI-film/BOX. Here a significantly higher number of defects (CDF) may be expected than in type B at the interface BOX/Si substrate where the oxide has been thermally grown and CDS-type defects are located. In type B the defect densities should be the other way round.

The bonding step in the Smart Cut process may cause the formation of defects at the bonded interface in the SOI-wafer. The reason is the formation of water during this step which leads to expansion and therefore to the formation of defects, e.g., tiny bubbles, in one of the two interfaces [111].

Red spots were not observed after copper decoration via electrochemical copper deposition out of a $Cu(NO_3)_2$ spiked dilute hydrofluoric acid solution. This result supports the assumption of the origin of the red spots as defects in one of the two interfaces. Copper decoration via electrochemical deposition occurs at the SOI surface. Here metallic copper is deposited on the surface at room temperature and does not move to the interface whereas in the case of

copper decoration via furnace annealing the copper diffuses from the back of the wafer fragment through the whole substrate and the interfaces to the SOI film.

3.7.1 Copper decoration and etching of crystal defects in standard SOI with different layer thicknesses

Further copper decoration studies were performed on different standard SOI materials to improve and refine the decoration parameters. The SOI films used were of different thicknesses: 62, 90, 118 and 149 nm, the thickness of the buried oxide (BOX) was 145 nm in all cases.

For copper decoration $Cu(NO_3)_2$ solutions in the concentration range from 0.0001-1 ppm (weight) corresponding to 1.57 x 10^{-9} to 1.57 x 10^{-5} mol/L of $Cu(NO_3)_2$ were used and, to prevent copper cross contamination in the furnace, the precautions outlined in chapter 3 were taken. After copper decoration the SOI fragments were etched either with dilute Secco (0.04 M Cr (VI)) or OPE D (composition: 50% H_2O_2, 50% HF, 100% propanoic acid) from their initial layer thickness down to approx. 20-70 nm (22-47% as residual layer thickness). The samples were treated with a dip in HF for approx. 90 s after etching with dilute Secco (0.04 M Cr (VI)). A dip in HF is not necessary after etching with OPE D. Selected defects were analyzed via SEM and AFM. The defect densities of copper decorated SOI fragments were compared with non-decorated fragments ("references"):

- After etching by a dilute Secco (0.04 M Cr (VI)) called "virgin" fragments (Ref 1)
- After furnace annealing without copper decoration followed by etching (Ref 2)

Copper decoration and preferential etching with dilute Secco (0.04 M Cr (VI))

Tab. 3.3 shows the average of defect densities for SOI fragments with layer thicknesses of 62, 90, 118 and 149 nm for non-decorated references (Ref 1 and Ref 2) and selected copper concentrations. Characteristic defect densities for SOI references are about D_{mean} = 1 100-8 200 cm^{-2} (Ref 1) and approx. D_{mean} = 2 300-13 500 cm^{-2} (Ref 2), and for copper decorated samples D_{mean} = 3 300-19 500cm^{-2} (0.001 ppm of copper) and D_{mean} = 7 000-21 900 cm^{-2} (1 ppm of copper). The average residual layer thicknesses (LT) of the samples are presented in Tab. 3.4.

Tab. 3.3 Comparison of average DD after Secco etching.

Conc. of Cu [ppm]	$\overline{DD}_{62\ nm}$ [cm^{-2}]	$\overline{DD}_{90\ nm}$ [cm^{-2}]	$\overline{DD}_{118\ nm}$ [cm^{-2}]	$\overline{DD}_{149\ nm}$ [cm^{-2}]
Ref 1	DD_{mean} 6 500 DD_{max} 22 600 DD_{min} 0	DD_{mean} 8 200 DD_{max} 19 800 DD_{min} 2 800	DD_{mean} 1 700 DD_{max} 5 600 DD_{min} 0	DD_{mean} 1 100 DD_{max} 5 600 DD_{min} 0
Ref 2	DD_{mean} 13 500 DD_{max} 28 200 DD_{min} 2 800	DD_{mean} - DD_{max} - DD_{min} -	DD_{mean} 3 100 DD_{max} 14 100 DD_{min} 0	DD_{mean} 2 300 DD_{max} 14 100 DD_{min} 0
0.001	DD_{mean} 9 600 DD_{max} 19 800 DD_{min} 0	DD_{mean} 19 500 DD_{max} 31 100 DD_{min} 11 300	DD_{mean} 6 400 DD_{max} 25 400 DD_{min} 0	DD_{mean} 3 300 DD_{max} 14 100 DD_{min} 0
1	DD_{mean} 21 900 DD_{max} 50 800 DD_{min} 2 800	DD_{mean} 21 300 DD_{max} 53 600 DD_{min} 2 800	DD_{mean} 11 400 DD_{max} 59 300 DD_{min} 0	DD_{mean} 7 000 DD_{max} 22 600 DD_{min} 0

Tab. 3.4 Residual layer thicknesses (LT) of etched fragments and corresponding copper concentrations.

Conc. of Cu [ppm]	$LT_{62\ nm}$ [nm]	$LT_{90\ nm}$ [nm]	$LT_{118\ nm}$ [nm]	$LT_{149\ nm}$ [nm]
Ref 1	22.30	33.61	51.74	67.59
Ref 2	23.04	-	50.47	65.34
0.001	18.60	19.26	46.02	60.83
1	20.04	25.22	45.19	59.60

Fig. 3.32 is a diagram to illustrate the ratios of DD of copper decorated and non-decorated (Ref 1 and Ref 2) samples with an initial SOI-film layer thickness of 118 nm. After furnace treatment without copper decoration (Ref 2) the defect densities are higher compared to the non-annealed reference samples (Ref 1). Copper decoration leads to a significant increase in defect densities. The higher the copper concentration used, the higher the obtained defect densities (1 ppm of copper results in the highest DD).

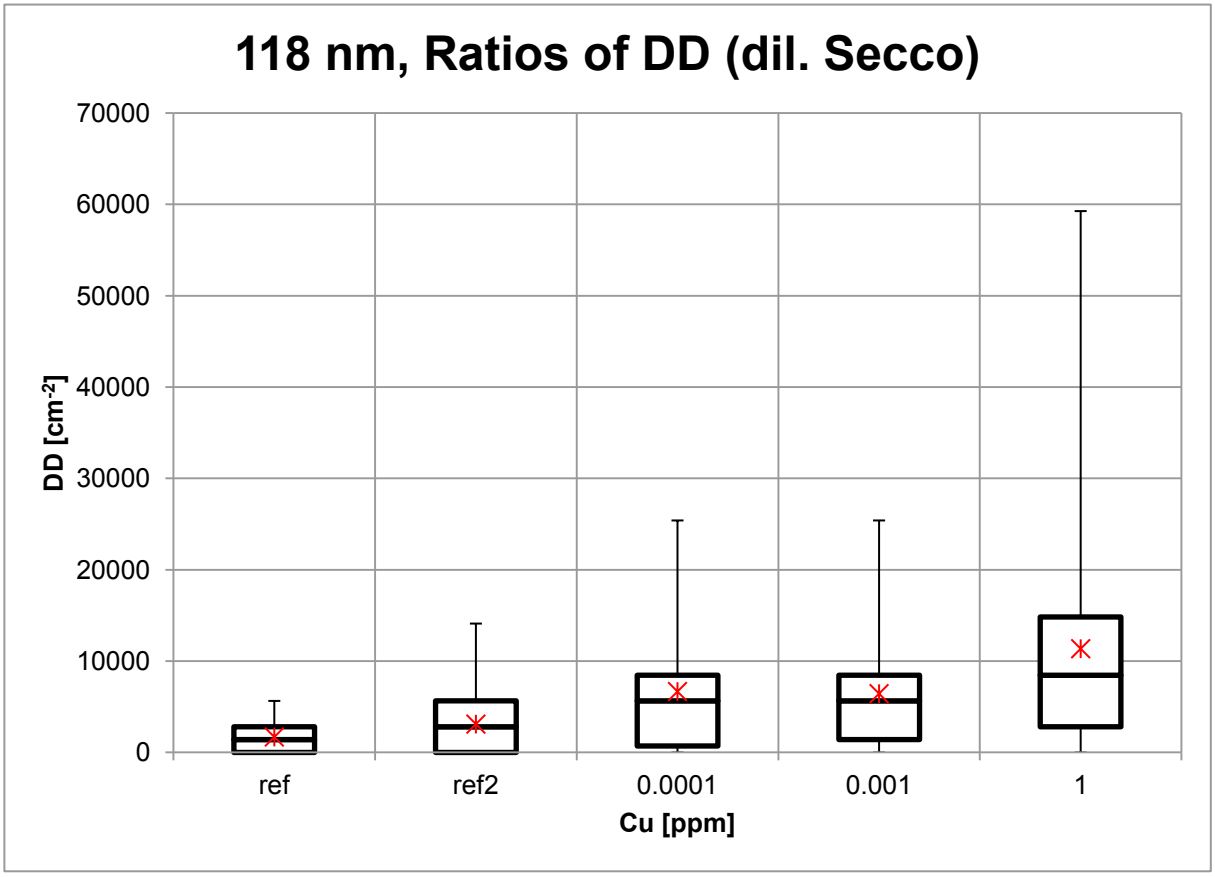


Fig. 3.32 Ratios of DD of Cu decorated and reference samples.

Fig. 3.33 gives an overview of defect densities and error bars of samples with SOI in all the thicknesses studied.

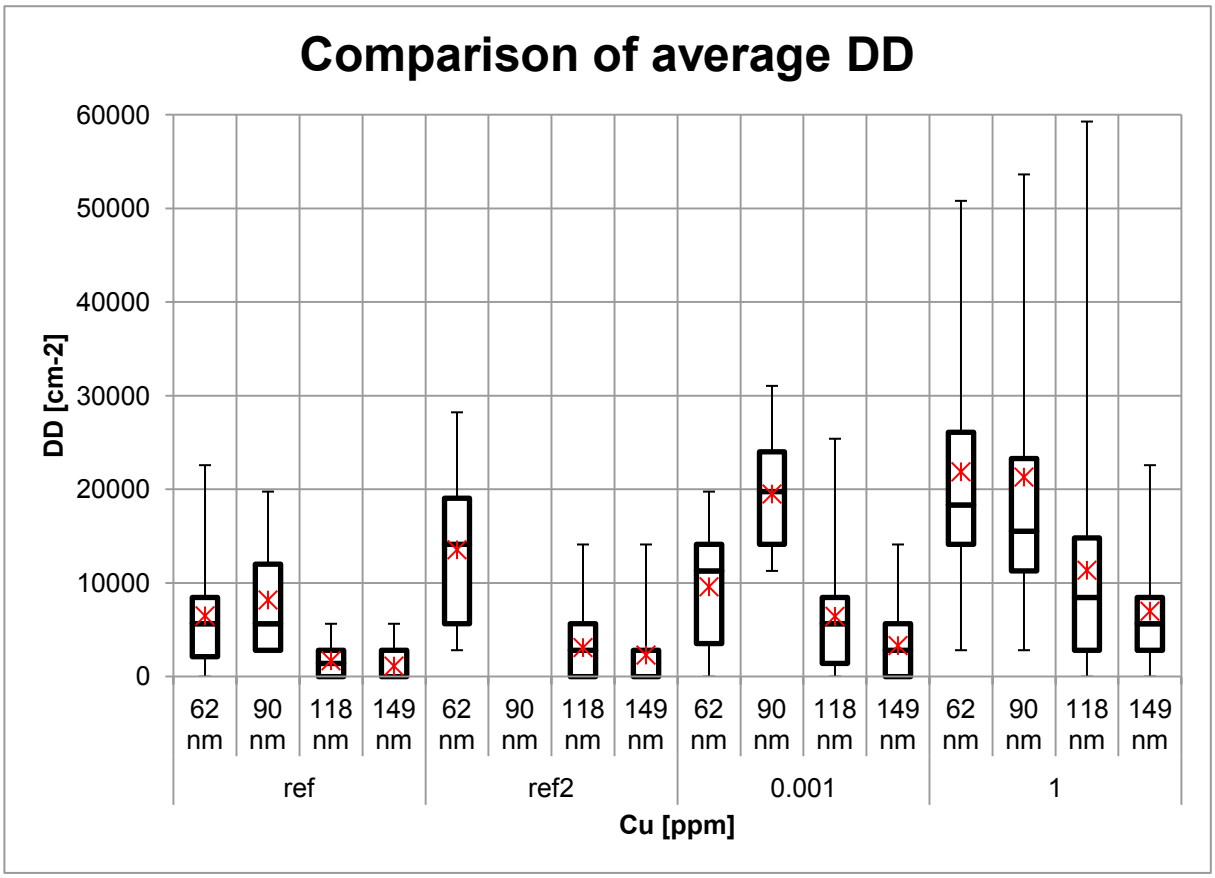


Fig. 3.33 Ratios of DD and error bars of 62-149 nm SOI samples after Secco etching. Ref 1 and Ref 2 (149 nm): Sharp distribution close to detection limit.

The following results were obtained after these decoration experiments:

- **Increase of defect densities after a furnace treatment without copper decoration (Ref 2)**

  The DD of Ref 2 is about twice as high as the DD of Ref 1. During the annealing process small defects, in particular oxygen precipitates, may grow due to the high temperatures in the furnace and may contribute to the defects detected after etching. A further contribution may come from the copper cross contamination in the furnace.

- **After copper decoration there is a significant increase in defect densities.**

  The higher the copper concentration, the higher the defect density obtained. This may be attributed to small defects decorated by the copper which are not otherwise detected by Secco etching. Copper leads to an increase of the etch rate. Therefore more defects which protrude down to the BOX and more defects with a halo are detected after etching. The DD obtained after decoration with 1 ppm of copper is higher than that determined after decoration with 0.001 ppm. One reason might be that not enough copper is available in the case of the low copper concentration to

decorate all small defects. Moreover, copper precipitation induced artefacts could also have contributed to the high DD obtained with 1 ppm of copper.

- **Decrease of defect densities with increasing SOI film thickness**

  The defects in a SOI film are distributed across in the whole layer. The residual layer thickness of thinner SOI layers (62 and 90 nm) was about 18–34 nm and that of the thick SOI layers (118 and 149 nm) was about 42–70 nm (Tab. 3.4). However, the defects in the deeper parts of the 118 and 149 nm SOI fragments seemed not to be reached by Secco etching. Just the defects in the upper part of these fragments are delineated by the etching process. For thicker residual layers part of the etch pits do not protrude down to the BOX and, hence, no halo is formed in the subsequent HF dip. Consequently, the DD determined for the 118 and 149 nm SOI fragments is lower compared to the 62 and 90 nm SOI.

A small increase in the etch rate of the dilute Secco (0.04 M Cr (VI)) was observed after furnace annealing and copper decoration.

An etch pit with a halo of a defect in a Ref 1 SOI fragment is shown in Fig. 3.34 with an initial SOI-film layer thickness of 118 nm which offers a low defect density (DD: 450 cm^{-2}).

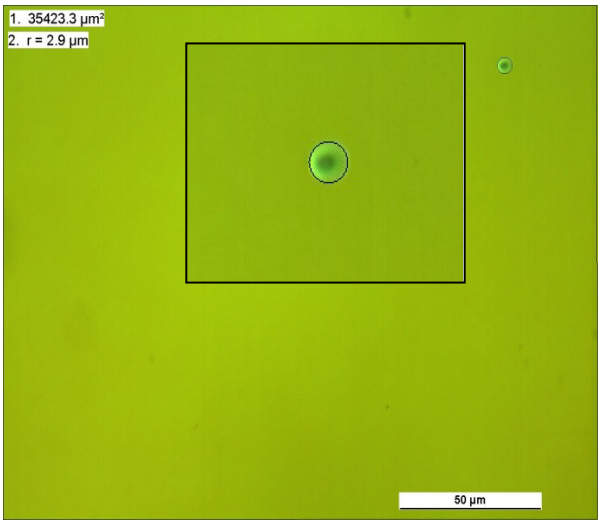


Fig. 3.34 Light optical micrograph of a "virgin" 118 nm SOI Ref 1 sample, etched with dilute Secco (0.04 M Cr (VI)), dipped in HF for 90 s. Residual layer thickness: approx. 52 nm, DD: 450 cm^{-2}.

Fig. 3.35 shows copper decorated SOI fragments (0.0001 ppm Cu (left image) and 1 ppm Cu (right image) with an initial SOI-film layer thickness of 118 nm. Compared to the reference sample of the same wafer the defect density in both images is higher. Whereas the defect density of the SOI fragment which is copper decorated with 1 ppm (DD: 16 300 cm^{-2}) is still higher than the defect density of the 0.0001 ppm (DD: 6 200 cm^{-2}) decorated fragment. The

possible copper precipitation induced artefacts seem to get minimized or even get prevented after reducing the used copper concentration while decorating even small defects not detected by Secco etching without copper decoration. In Fig. 3.35 “red spots” [110] are visible (see above for explanation). These “red spots” appeared in some of the analyzed copper decorated SOI fragments of these wafers.

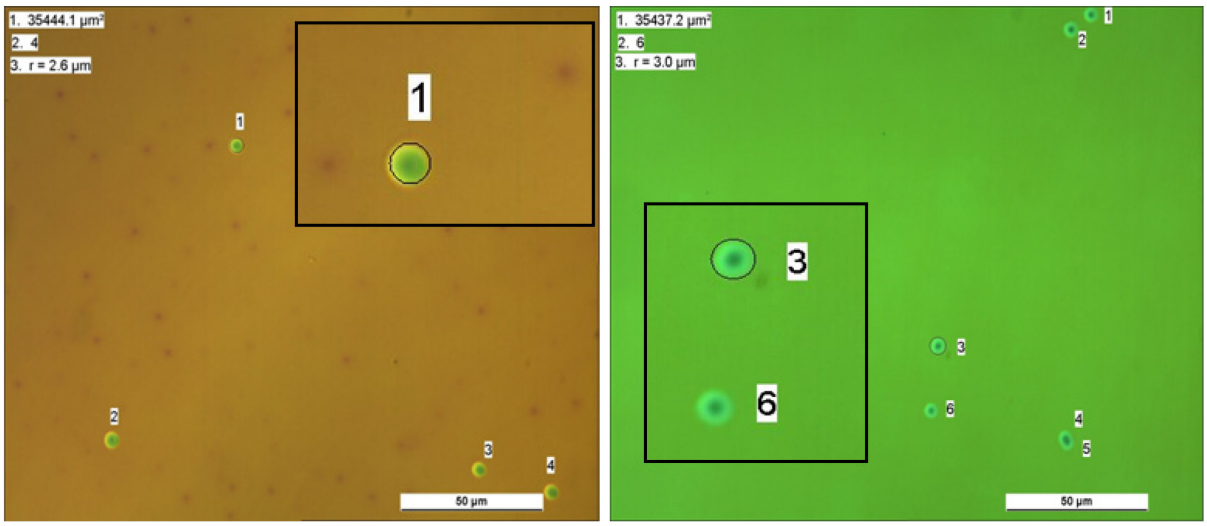


Fig. 3.35 Light optical micrographs of 118 nm SOI samples, decorated with 0.0001 ppm of Cu (left) and 1 ppm of Cu (right), annealed at 800 °C, etched with dil. Secco (0.04 M Cr) and dipped in HF for 90 s. DD left: 6 200 cm^{-2}, DD right: 16 300 cm^{-2}, residual layer thickness: approx. 50 nm.

Copper decoration and preferential etching with OPE D

Standard SOI samples of 118 and 149 nm SOI layer thickness were decorated with 0.0001, 0.001 and 1 ppm of copper and etched with an OPE D etching solution (see appendix 6.1 for composition). A comparison was made of the densities and appearance of the defects between

- Non - decorated references (Ref 1 and Ref 2) and copper decorated fragments etched with OPE D
- Samples after decoration and etching with OPE D and those decorated and etched with the dilute Secco (0.04 M Cr (VI))

Tab. 3.5 presents the DD obtained for reference (Ref 1 and Ref 2) and copper decorated samples. The fragments were etched for 39 min at room temperature (23 °C). A dip in HF was not necessary for the delineation of the defects. The residual layer thicknesses are shown in Tab. 3.6.

Tab. 3.5 Comparison of average DD after OPE D etching.

Conc. of Cu [ppm]	$\overline{DD}_{118\ nm}$ [cm^{-2}]	$\overline{DD}_{149\ nm}$ [cm^{-2}]
Ref 1	DD_{mean} 3 100 DD_{max} 8 500 DD_{min} 0	DD_{mean} 6 800 DD_{max} 16 900 DD_{min} 0
Ref 2	DD_{mean} 11 600 DD_{max} 25 400 DD_{min} 0	DD_{mean} 18 100 DD_{max} 39 500 DD_{min} 0
0.0001	DD_{mean} 10 000 DD_{max} 31 100 DD_{min} 0	DD_{mean} 4 100 DD_{max} 16 900 DD_{min} 0
0.001	DD_{mean} 14 400 DD_{max} 33 900 DD_{min} 0	DD_{mean} 7 900 DD_{max} 22 600 DD_{min} 0
1	DD_{mean} 23 400 DD_{max} 64 900 DD_{min} 0	DD_{mean} 14 800 DD_{max} 36 700 DD_{min} 0

Tab. 3.6 Residual layer thicknesses (LT) of etched fragments and corresponding copper concentrations.

Conc. of Cu [ppm]	$LT_{118\ nm}$ [nm]	$LT_{149\ nm}$ [nm]
Ref 1	54.75 ± 1.61	71.30 ± 1.80
Ref 2	50.79 ± 1.31	63.85 ± 1.82
0.0001	50.54 ± 1.02	63.88 ± 0.48
0.001	53.99 ± 1.41	67.45 ± 0.84
1	51.89 ± 0.90	65.88 ± 0.35

Tab. 3.5 and Fig. 3.36 show that the DD of the Ref 2 samples are 3–4 times higher than those of the Ref 1 samples. Annealing may cause the precipitation of interstitial oxygen at already existing oxygen nuclei sites thus producing larger, detectable defects. The much higher DD is also an indication of the high efficiency of OPE D in delineating defects.

The DD did not increase after decoration with 0.0001 and 0.001 ppm of copper (D_{mean} =4 100–14 400 cm^{-2}) compared to the Ref 2. Decoration with 1 ppm of copper leads to an increase in DD (D_{mean} = 14 800–23 400 cm^{-2}) over non-decorated samples or those decorated with a low concentration of copper. Either the decoration of the defects occurs at a copper concentration of 1 ppm of copper or the higher DD can be attributed to artefacts induced by copper precipitation.

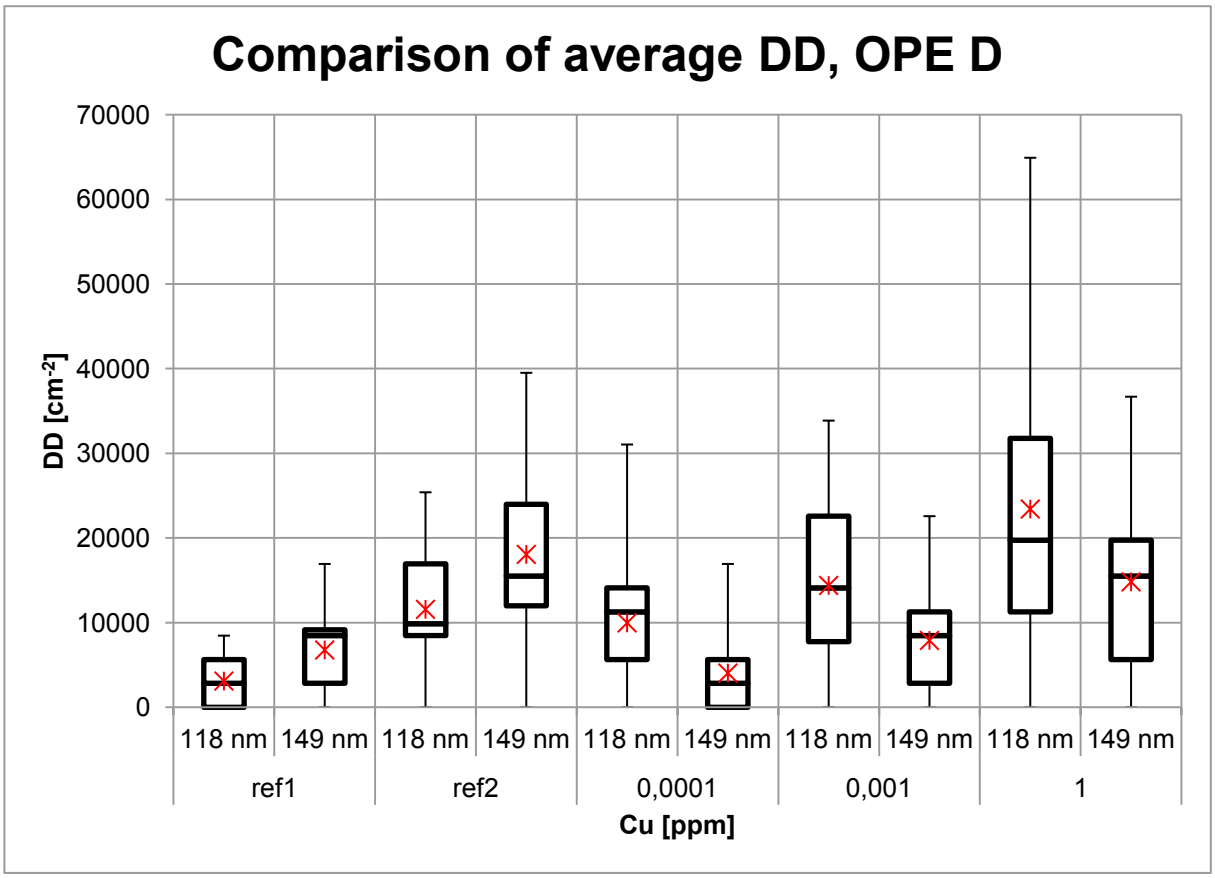


Fig. 3.36 Comparison of the average DDs of reference and copper decorated fragments with 118 nm and 149 nm thick SOI film after OPE D etching (see Tab. 3.5).

Fig. 3.37 shows a light optical micrograph of a Ref 1 sample. The radii of the halos of the defects vary considerably, the average radii ranging from 1.13–9.29 µm. Both defects in Fig. 3.37 have a circular shape but differ in their radius (r_1 = 2.1 µm and r_2 = 5.7 µm). The average radii of the defects measured after etching with OPE D are larger than the radii of the defects determined after etching with a dil. Secco etch. Removal rate of OPE D on Smart Cut SOI is 1.7 ± 0.12 nm/min [112], that of Secco dil. (0.04 M Cr (VI)) is 0.65 nm ± 0.25 nm/s. This comparatively low etch rate requires that the samples to be etched much longer. The result is larger radii of the halos in the upper part of the SOI film. Moreover, OPE D contains a considerable amount of HF which is why the BOX gets etched without the additional dip in HF. Defect size and depth from the surface in the layer determines the size of the halo. The small etch pits could be at defects which occur deeper in the SOI film and etched by the more sensitive and HF containing OPE D. The longer the sample remains in OPE D the larger the halo.

The radii of the defects are comparable with those after etching with a dil. Secco (0.04 M Cr (VI)) (average radii: 2.45–3.95 µm). However, in contrast to the dil. Secco (0.04 M Cr (VI)), the OPE D solution appears to reach defects that lie deeper in the SOI film.

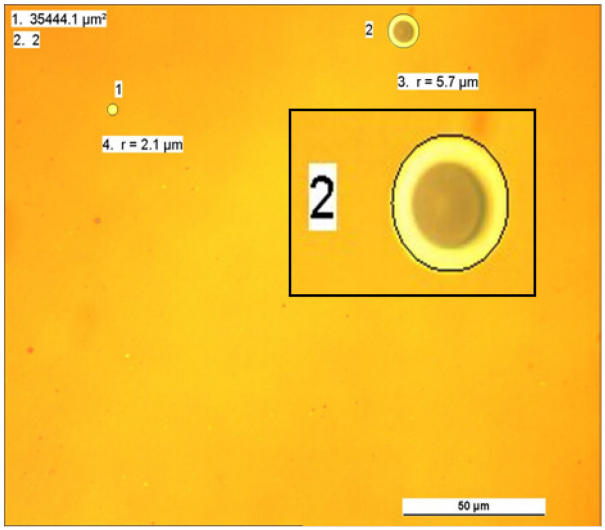


Fig. 3.37 Light optical micrograph of a 118 nm Ref 1 sample; etched with OPE D, residual layer thickness: approx. 55 nm, magnification: 500x. Defects are delineated as circular pits with halo. See Furnace annealing for explanation of red spots.

Fig. 3.38 shows a light optical micrograph of a Ref 2 sample. The defects have the same circular shape but they differ in their radii (r_1 = 0.9 µm and r_2 = 6.3 µm). Furthermore, red spots could be detected in a few samples (see magnified view). The density of small-sized defects increases after the annealing step.

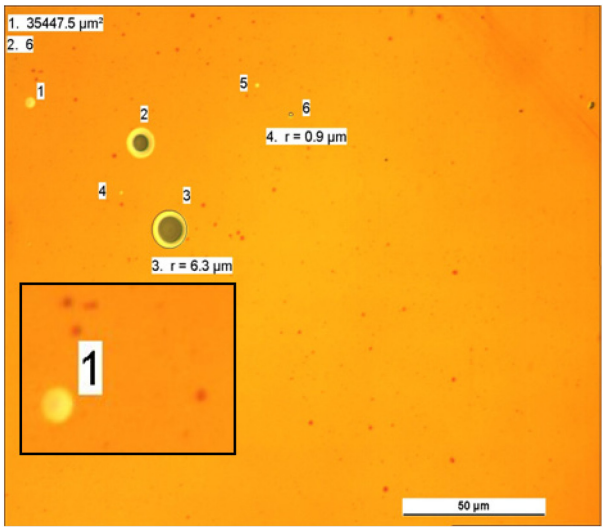


Fig. 3.38 Light optical micrograph of a 118 nm Ref 2 sample, etched with OPE D, residual layer thickness: approx. 51 nm, magnification: 500x. Defects are delineated as circular pits with halo.

A SOI sample decorated with 1 ppm of copper and etched with OPE D is presented in Fig. 3.39. The DD is higher than that of the references. Many defects have a small radius. All small defects have a bright halo. These are defects with an almost completely preserved SOI layer at the defect. The decorated larger defects differ in their appearance from the non-

decorated ones. They are very dark as the SOI film has sunk to the bottom of the etch pit which is the silicon substrate. There is hardly any bright halo.

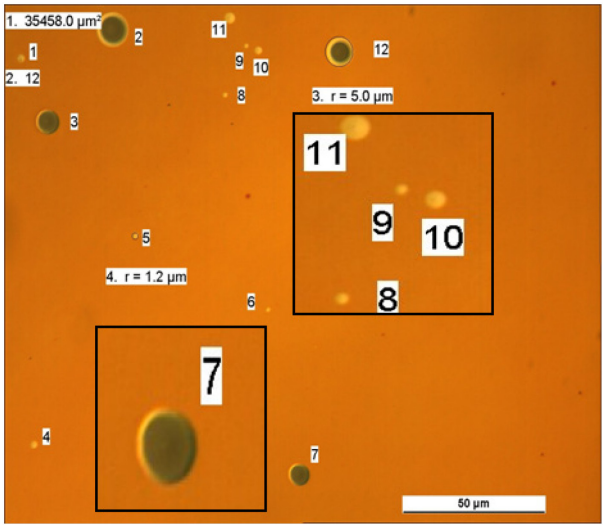


Fig. 3.39 Light optical micrograph of a 118 nm sample decorated with 1 ppm Cu, annealed for 1 min. at 800 °C, etched with OPE D , residual layer thickness: approx. 52 nm, magnification: 500x.

Fig. 3.40 and Fig. 3.41 allow a comparison between DDs obtained with dil. Secco (0.04 M Cr (VI)) and those obtained with OPE D. The DD of copper decorated samples are consistently higher in the OPE D etched samples. OPE D etching could have also revealed small oxygen precipitates (“oxygen nuclei”) while dil. Secco (0.04 M Cr (VI)) could either not, or only partially be capable of revealing them.

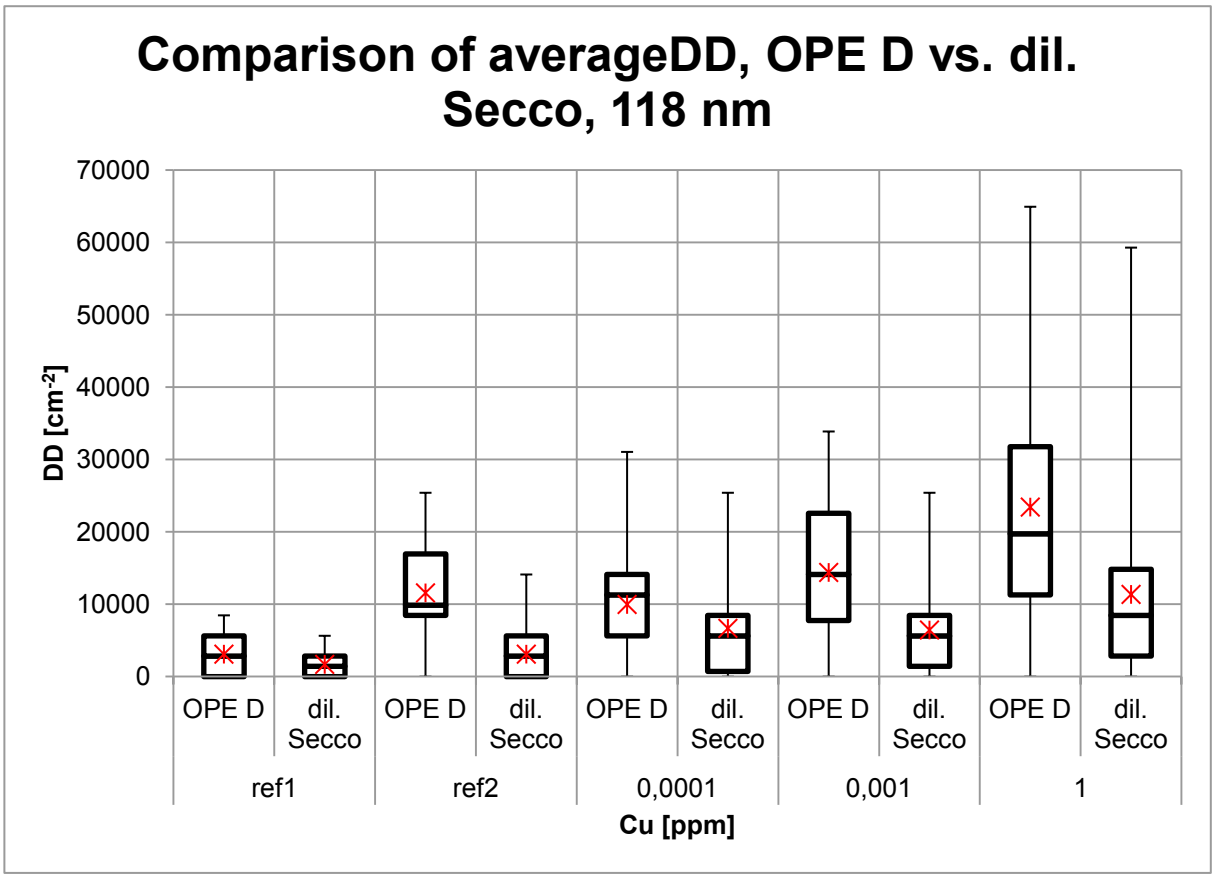


Fig. 3.40 Comparison of the average DD of non-decorated and Cu-decorated 118 nm SOI fragments etched with OPE D and a dil. Secco (0.04 M Cr (VI)).

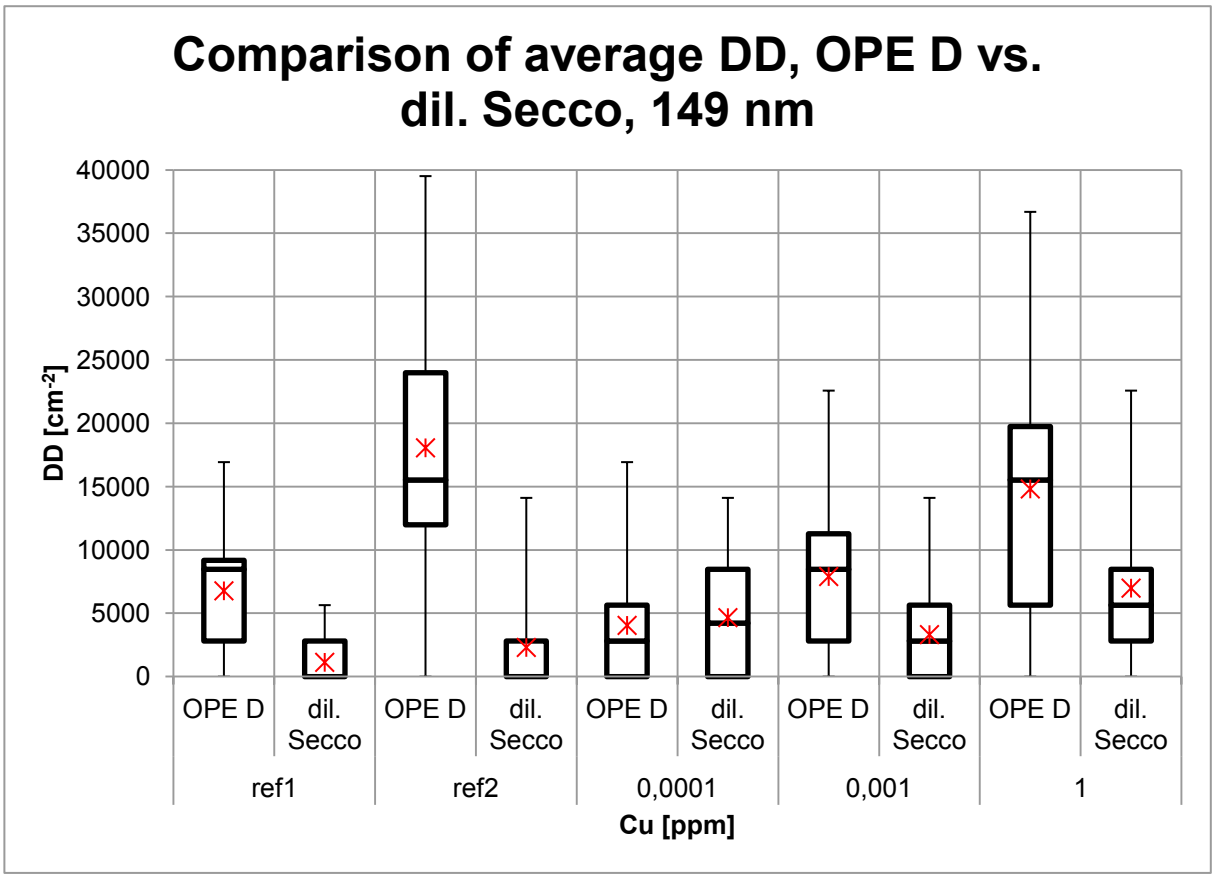


Fig. 3.41 Comparison of the average DD of non-decorated and Cu-decorated 149 nm SOI fragments etched with OPE D and a dil. Secco (0.04 M Cr (VI)).
Ref 1 and Ref 2 (dil. Secco): Sharp distribution close to detection limit.

3.7.2 Decoration of Oxygen induced Stacking Faults (OiSF) in standard SOI

Oxidation **i**nduced **S**tacking **F**aults (OiSF) are crystal defects which are formed in the SOI fabrication process during the oxidation step of the SOI wafers for smoothing of the SOI film surface. OiSF start to grow all at the same time at the beginning of the oxidation process. They can be revealed by different preferential etching solutions such as dilute Secco.

In the course of improving the SOI process at SOITEC, SOI material was produced which contained an unusually large amount of OiSFs. Samples of this material were used to study decorated OiSF.

The SOI-films used had an initial layer thickness of 90.7 nm, the thickness of the BOX was 145 nm. After copper decoration the SOI fragments were etched with dilute Secco (0.04 M Cr (VI)) to a layer thickness of approx. 45 nm. Most of the fragments were treated with a dip in HF for approx. 45 s to delineate the defects. Some were analysed without a dip, a few with a dip of only 15 seconds. Selected defects were also inspected via SEM and AFM. The defect

densities of copper decorated OiSF were compared with those of non-decorated ones (Ref 1 and Ref 2).

Tab. 3.7: DD of OiSF of non-decorated references (Ref 1, Ref 2) and Cu decorated samples.

Cu [ppm]	DD [cm^{-2}]
Ref 1	DD_{mean} 1 100 DD_{max} 11 300 DD_{min} 0
Ref 2	DD_{mean} 2 300 DD_{max} 11 300 DD_{min} 0
0.0001	DD_{mean} 2 300 DD_{max} 11 300 DD_{min} 0
0.001	DD_{mean} 2 800 DD_{max} 11 300 DD_{min} 0
0.01	DD_{mean} 7 400 DD_{max} 11 300 DD_{min} 0
0.1	DD_{mean} 6 200 DD_{max} 11 338 DD_{min} 0
1	DD_{mean} 8 500 DD_{max} 11 300 DD_{min} 0

Tab. 3.7 and Fig. 3.42 show that the defect densities of OiSF for annealed references are twice as high as those of the non-annealed references although an increase should not be

expected. However, during annealing, interstitial oxygen could have precipitated at oxygen nuclei which then grow in size and are detectable.

Copper decoration at concentrations of 0.0001 and 0.001 ppm of copper resulted in DD in the same range as the annealed Ref 2. DDs increased considerably at a concentration of 0.01ppm and did not increase much further at 1ppm. It is not clear why the DDs increased after copper decoration.

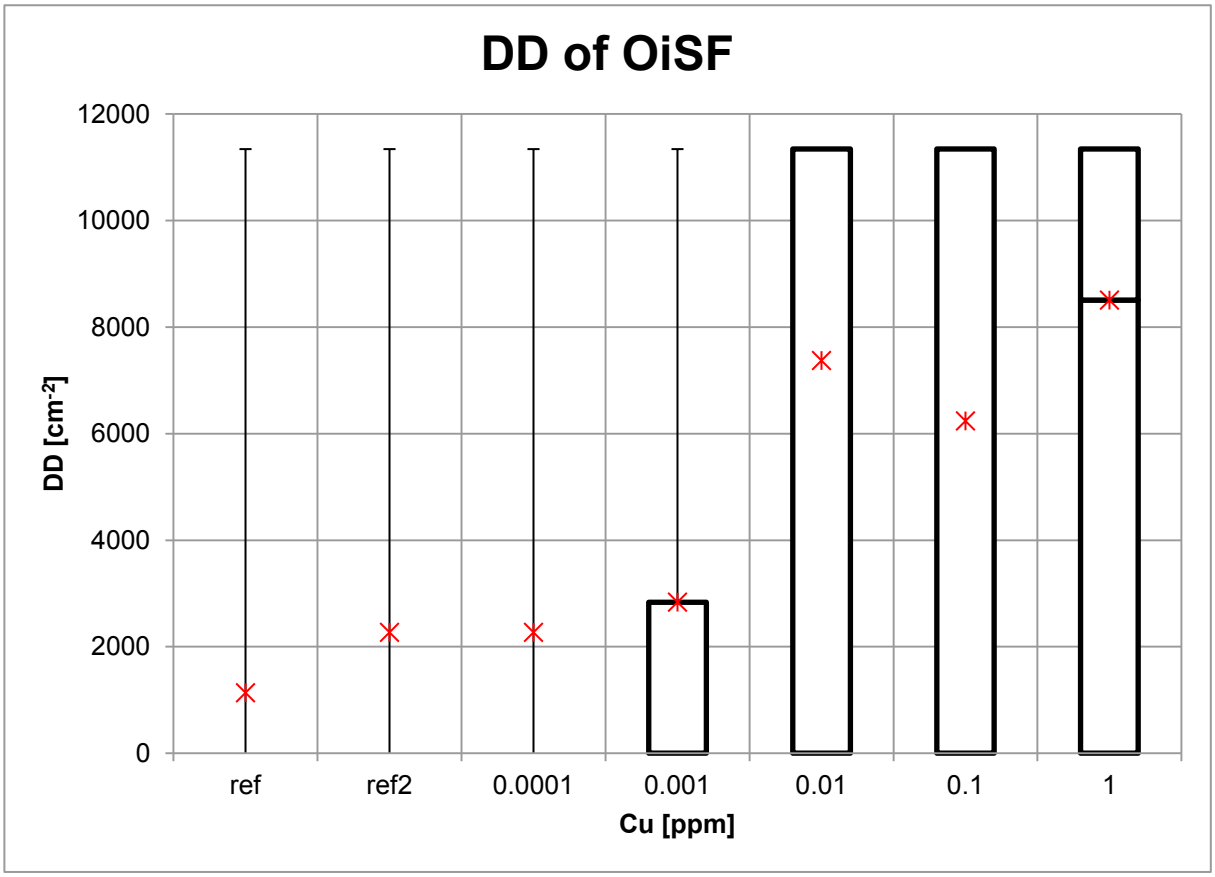


Fig. 3.42 DD of OiSF of non-decorated reference (Ref 1, Ref 2) and Cu decorated samples. Ref 1 Ref 2 and 0.0001 ppm Cu: Only few samples barely reaching detection limit. 0.01 and 0.1 ppm Cu: Sharp distribution close to detection limit. 1 ppm Cu: Samples barely reaching detection limit.

Fig. 3.43 shows the difference between an OiSF etch pit in a non-annealed non-decorated HF-treated sample (right) and one without the dip in HF (left). The HF treatment has produced a halo which facilitates the identification with a light optical microscope of the otherwise barely visible OiSF (left). The two pits in the etch feature are not equal in size, suggesting the presence of a metal contaminant in the larger defect.

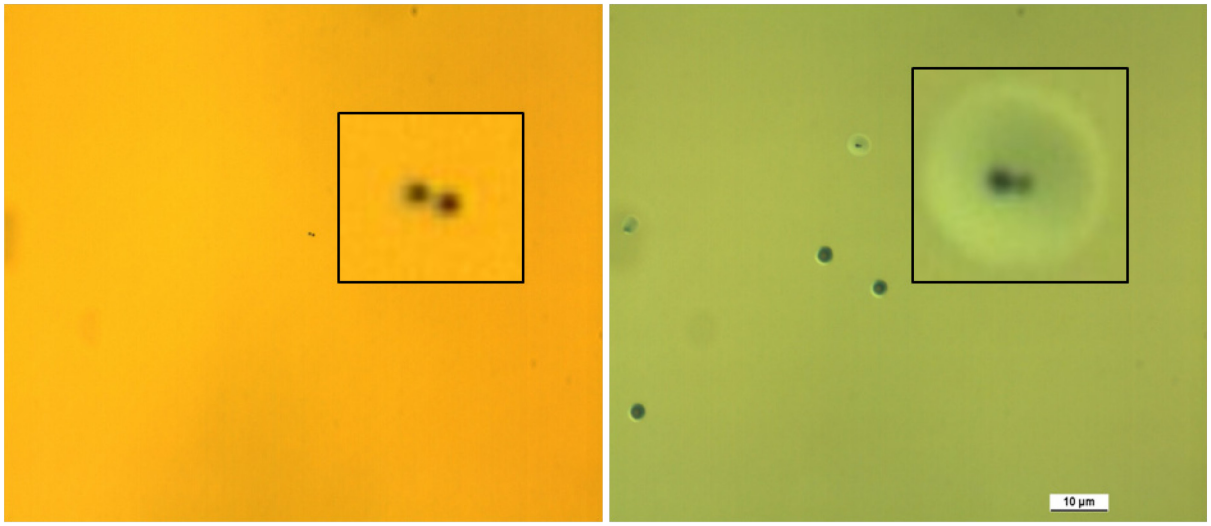


Fig. 3.43 Light optical micrograph of a 90.7 nm non-decorated and non-annealed reference SOI sample; etched with dil. Secco (0.04 M Cr (VI)); without a dip in HF (left) and with a dip in HF of 45 s (right); residual layer thickness in both images approx. 45 nm; OiSF visible. Magnified view inserted. Same magnification.

Fig. 3.44 shows two SEM images of undecorated OiSF (Ref 1) without a dip in HF (left) and after a dip in HF for 15 s (right). The 15 s dip in HF produced a halo, however it was not large enough to distinguish between the characteristic double pits of the OiSF from the single pits of other defects like COPs in a light optical micrograph. By this double pit feature OiSF can be discriminated unambiguously from other defects like COPs, oxygen precipitates and the like.

The characteristic form produced at an OiSF resembles a barbell. The two perforations originate from the partial dislocation binding the stacking fault and the line which connects them is an etched stacking fault. The perforation to the left of the stacking fault is again larger suggesting some degree of decoration due to metal contamination. The larger perforation also has a larger halo. The cause of the asymmetric behaviour of the partial dislocation is not known.

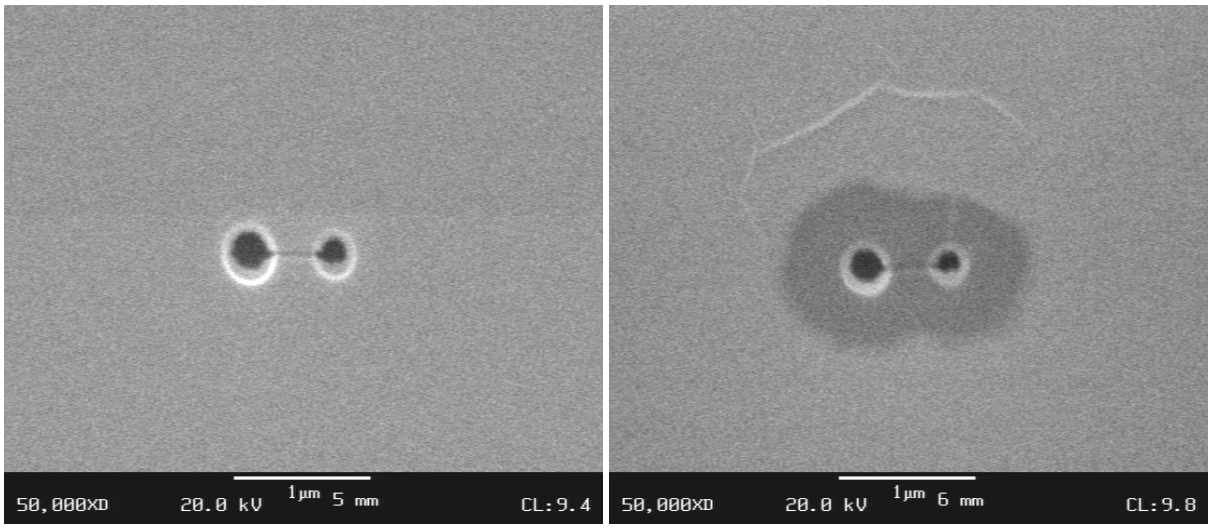


Fig. 3.44 SEM images of 90.7 nm Ref 1 SOI samples; etched with dil. Secco (0.04 M Cr (VI)); without a dip in HF (left), with a dip in HF of 15 s (right); residual layer thickness in both samples approx. 45 nm; OiSF visible.

Another SOI sample was etched and dipped in HF for 45 s (Fig. 3.45) followed by a closer inspection of OiSF via SEM (left image) and AFM (right image). The OiSF is surrounded by a large halo, easily detected under a light optical microscope. All further etching experiments included a dip in HF for 45 s except where for the sake of comparison a dip was omitted. The stacking fault between the perforations is clearly identified in both images.

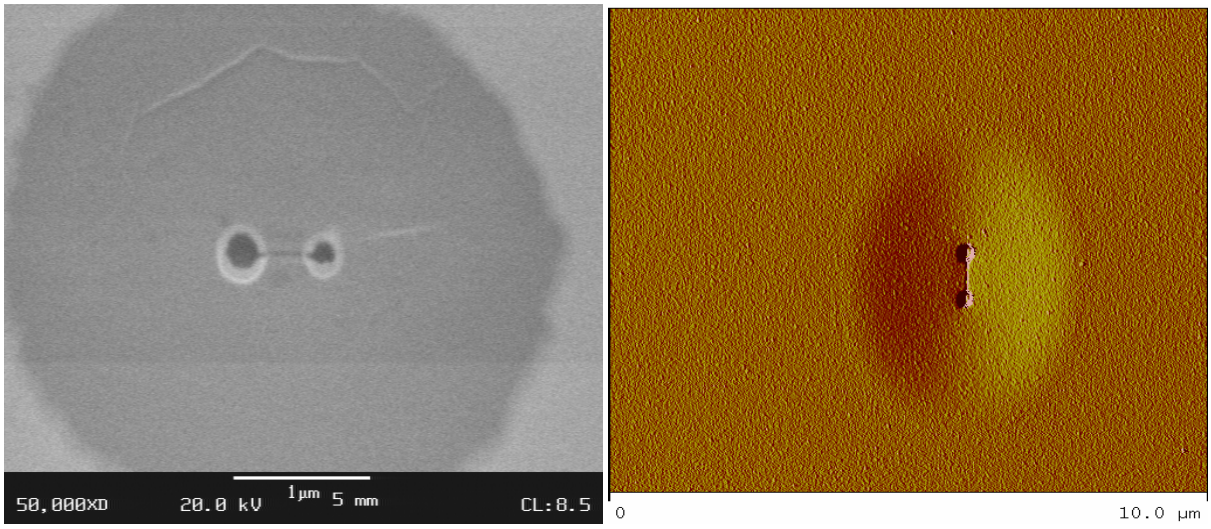


Fig. 3.45 SEM image (left), AFM image (right) of a 90.7 nm SO sample, Ref 1, etched with dil. Secco (0.04 M Cr (VI)) dipped in HF for 45 s; residual layer thickness approx. 45 nm; OiSF visible.

An AFM etch pit analysis of an undecorated OiSF (Ref 1) is presented in Fig. 3.46. The SOI layer collapsed at the double pit and a deep indentation is clearly visible in the section analysis.

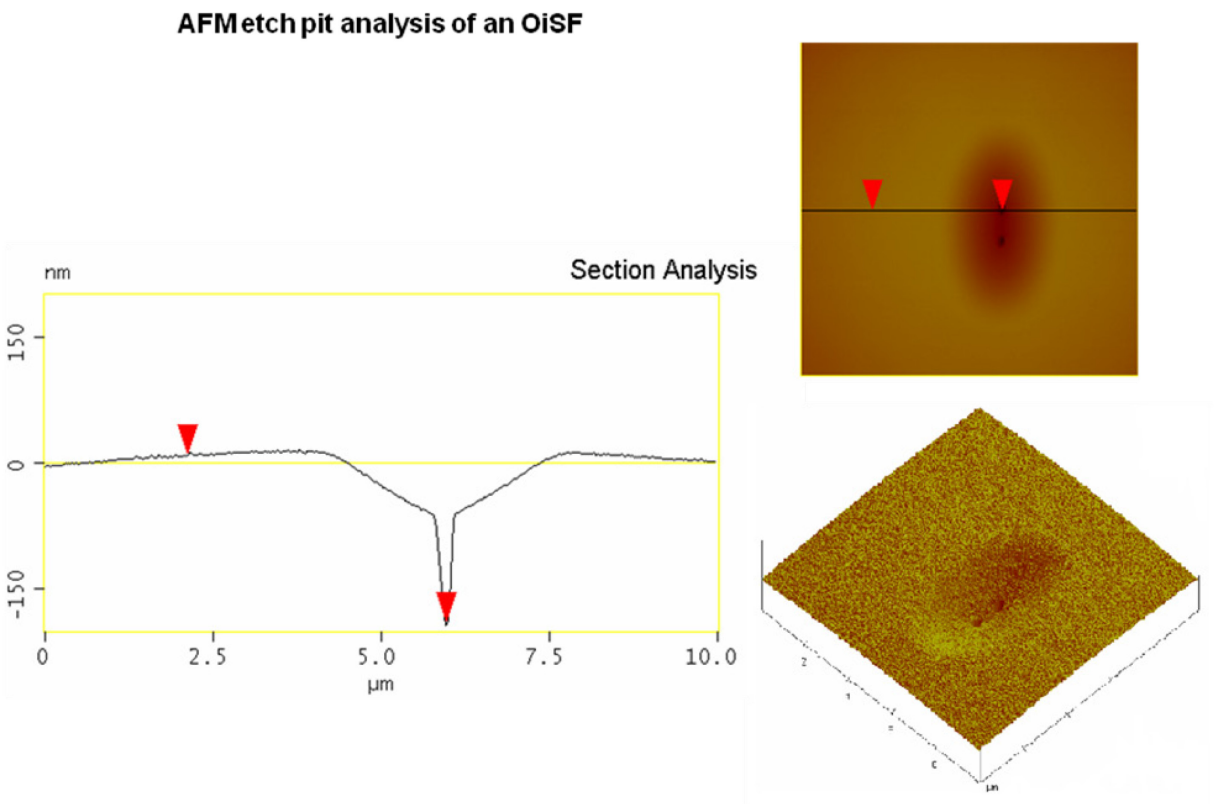


Fig. 3.46 AFM images and section analysis of a 90.7 nm Ref 1 SOI sample, etched with dil. Secco (0.04 M Cr (VI)), dipped in HF for 45 s; residual layer thickness approx. 45 nm; one OiSF visible.

The light optical micrograph of a Ref 2 sample presented in Fig. 3.47 shows pits with perforations that are equal in size in contrast to the non-annealed Ref 1. This may be induced by residual copper in the furnace used. The defects are of the same bright colour as the Ref 1. The SOI film collapsed after the HF dip.

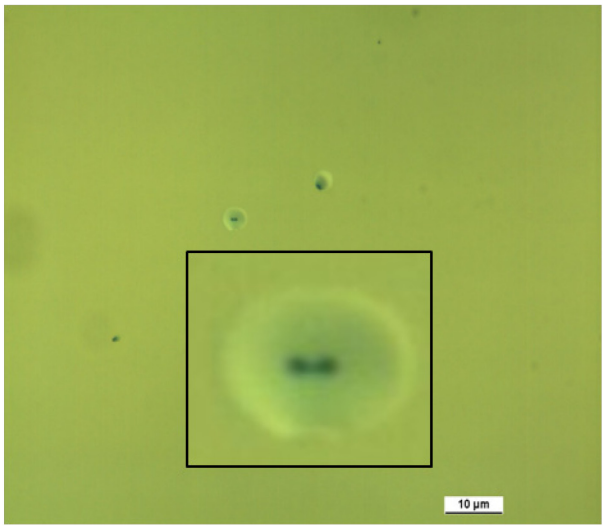


Fig. 3.47 Light optical micrograph of a 90.7 nm SOI Ref 2 sample; etched with dil. Secco (0.04 M Cr (VI)), dipped in HF for 45 s; residual layer thickness approx. 45 nm; one OiSF visible. Magnified view inserted.

Fig. 3.48 shows a light optical micrograph (left) and a SEM image (right) of a SOI sample which was copper decorated with a copper concentration of 0.0001 ppm and etched with a dilute Secco (0.04 M Cr (VI)) but not dipped in HF. The pits are similar in size.

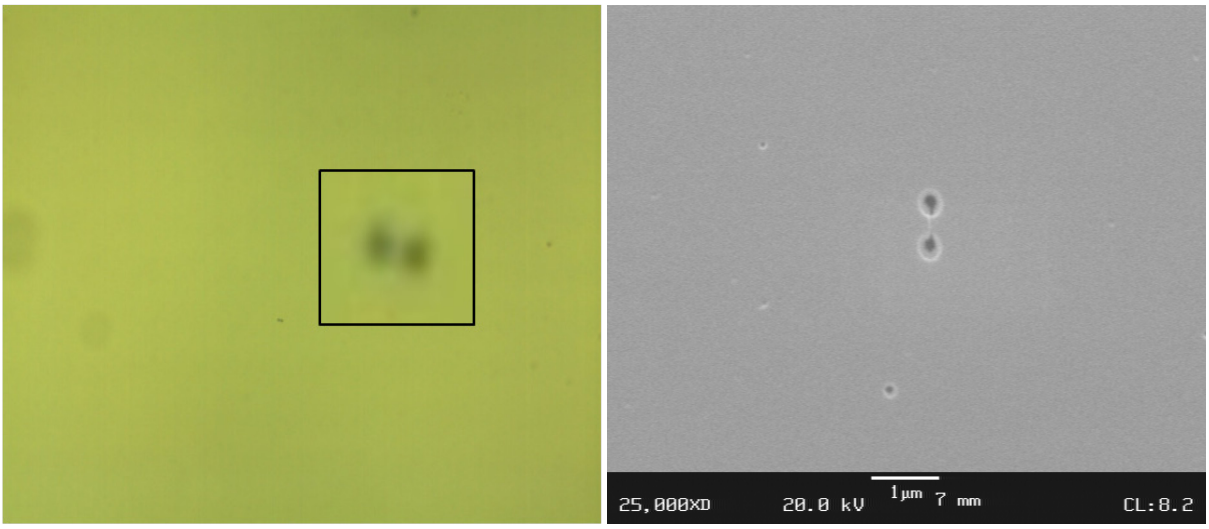


Fig. 3.48 Light optical micrograph (left) 1 000x, SEM image (right) of a 90.7 nm SOI sample; decorated with 0.0001 ppm Cu, annealed at 800 °C; etched with dil. Secco (0.04 M Cr (VI)), without a dip in HF, residual layer thickness: approx. 45 nm; OiSF visible.

Fig. 3.49 shows a copper decorated (0.0001 ppm Cu) and etched SOI sample with a subsequent dip in HF for 45 s. The left image is a light optical micrograph and the right one is a SEM of etch pits in the same sample. The pits are surrounded by a bright halo which is clearly visible in the light optical micrograph. There is no difference between the shape of these pits and those of the reference samples. The pits do not have the typical round shape of copper decorated etch pits.

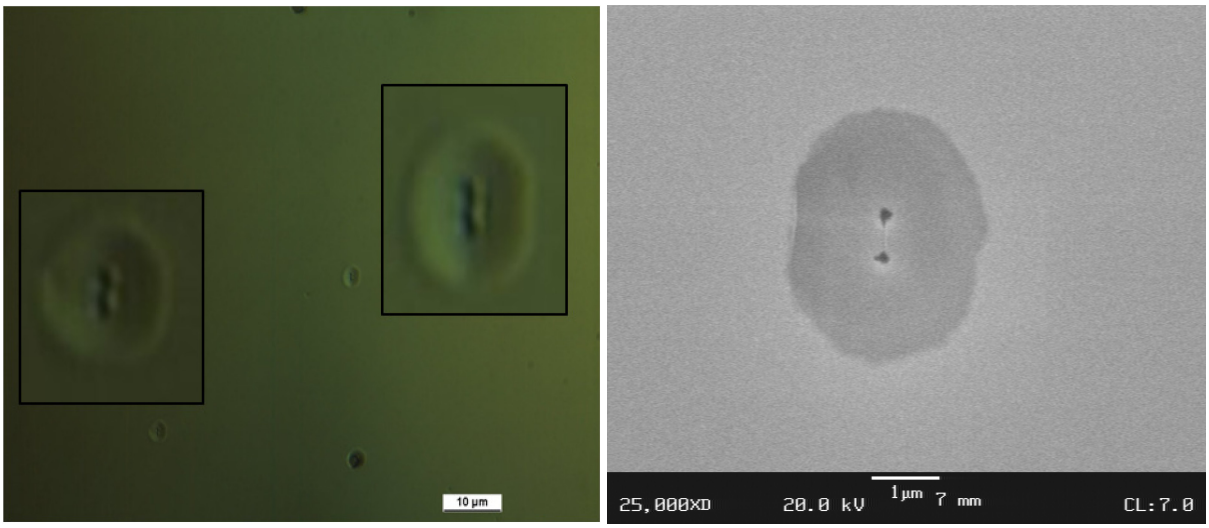


Fig. 3.49 Light optical micrograph (left), SEM image (right) of a 90.7 nm SOI sample; decorated with 0.0001 ppm Cu, annealed at 800 °C; etched with dil. Secco (0.04 M Cr (VI)), dipped in HF for 45 s; residual layer thickness approx. 45 nm; OiSF visible. Magnified view inserted.

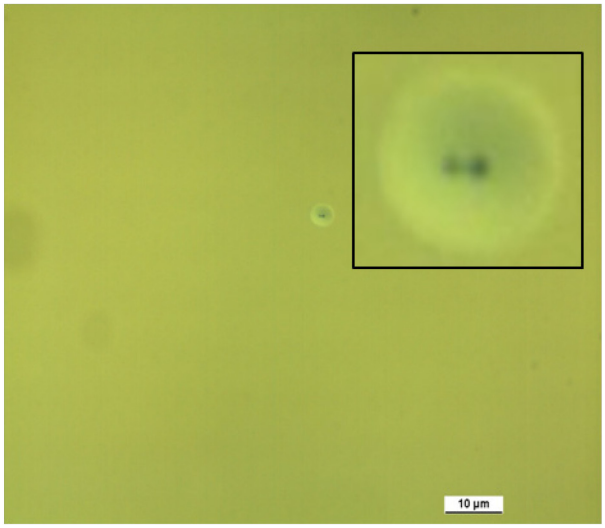


Fig. 3.50 Light optical micrograph of a 90.7 nm SOI sample, decorated with 0.001 ppm Cu, annealed at 800 °C; etched with dil. Secco (0.04 M Cr (VI)), dipped in HF for 45 s; residual layer thickness: approx. 45 nm; one OiSF visible. Magnified view inserted.

In Fig. 3.50 a SOI sample decorated with 0.001 ppm Cu and etched with dil. Secco with a subsequent dip in HF for 45 s is shown. Here, too, the pits are surrounded by a bright halo. However, there is no significant difference between these etch pits and those of non-decorated samples. The copper concentration was hence increased to 0.01ppm.

Fig. 3.51 shows the light optical micrograph of a SOI sample which was copper decorated with 0.01 ppm Cu and subsequently etched and dipped in HF for 45 s. The pits of the defect are surrounded by a halo with a dark nucleus and a bright circle. These etch pits differ completely from the non-decorated ones and resemble the copper decorated pits described

for other defects but with two perforations in the centre where the SOI has collapsed to the substrate. The bright halo is the inclined ring-like part of the SOI film at the defect while the dark area represents that part of the SOI film which collapsed to the substrate.

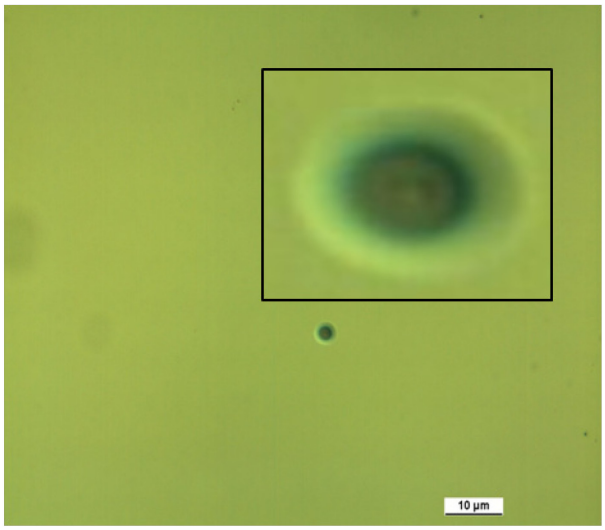


Fig. 3.51 Light optical micrograph of a 90.7 nm SOI sample; decorated with 0.01 ppm Cu, annealed at 800 °C; etched with dil. Secco (0.04 M Cr (VI)),dipped in HF for 45 s; residual layer thickness approx. 45 nm; magnification 1 000x; one OiSF visible. Magnified view inserted.

Two SEM images of OiSF are shown in Fig. 3.52. Both samples were just etched with a dil. Secco without a subsequent treatment in HF. The OiSF in the left image was not decorated and not annealed (Ref 1). The connection line between the two perforations of unequal size is clearly visible. The OiSF in the right SEM image is copper decorated (0.1 ppm Cu). The two perforations are about the same size and much bigger than those of the undecorated OiSF. The connecting stacking fault is “lost” under the perforations due to their enlargement, attributable to decoration with copper. The difference between a decorated and a non-decorated OiSF can be clearly seen in these two SEM images.

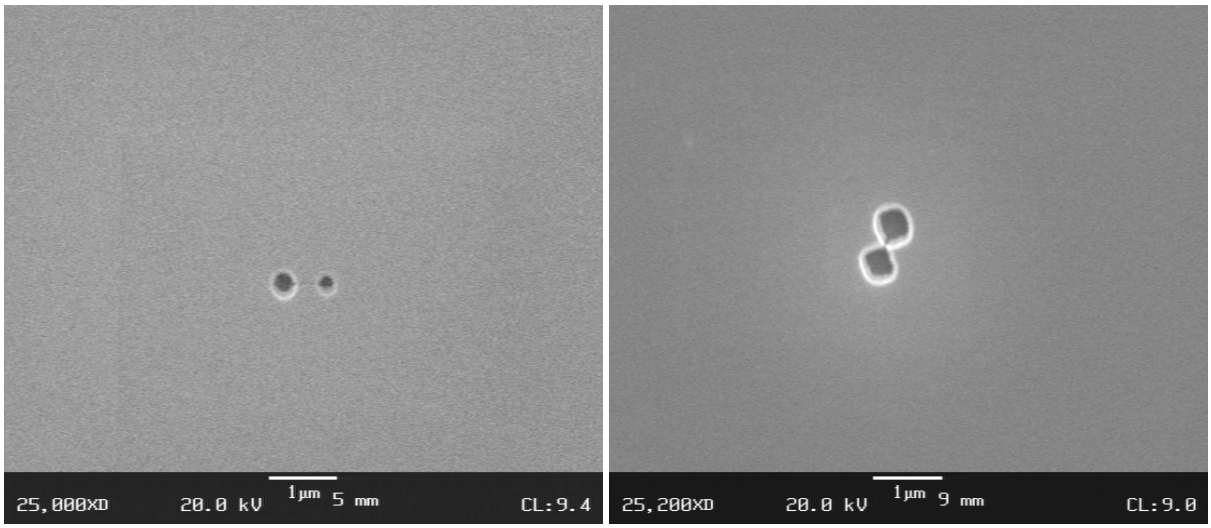


Fig. 3.52 SEM images of two 90.7 nm SOI samples; Ref 1 (left), decorated with 0.1 ppm Cu, annealed at 800 °C (right), both etched with dil. Secco (0.04 M Cr (VI)), without the dip in HF; residual layer thickness approx. 45 nm; one OiSF visible in each image.

Fig. 3.53 shows a copper decorated (0.1 ppm Cu) and etched OiSF which was dipped in HF for 45 s after etching, with a SOI film that has sunk to the bottom (dark circle) surrounded by a brighter circle of the inclined part of the residual SOI film. Copper has decorated this defect judging from the size of the pits and surrounding halo.

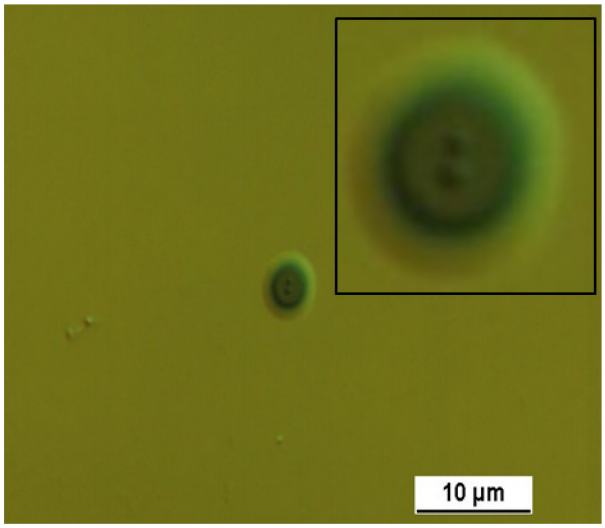


Fig. 3.53 Light optical micrograph of a 90.7 nm SOI sample, decorated with 0.1 ppm Cu, annealed at 800 °C; etched with dil. Secco (0.04 M Cr (VI)),dipped in HF for 45 s; residual layer thickness approx. 45 nm; one OiSF visible. Magnified view inserted.

Fig. 3.54 shows an optical micrograph (left) and an AFM image (right) of the pit of an OiSF decorated with 1 ppm Cu. The pits were clearly defined and easily identified as OiSF pits. However, there was no significant improvement in the shape and size of the pits over those of the pits produced with 0.1 ppm Cu. The DDs obtained remained in the same range as

those obtained with 0.1 ppm Cu. A concentration of 0.1 ppm Cu can therefore be regarded as sufficient for the delineation of OiSF. However, it must be noted that the area density of OiSF should not increase during the copper decoration process taking place at 800°C. As outlined at the beginning of this chapter the OiSF start to grow all at the same time at the beginning of the oxidation process.

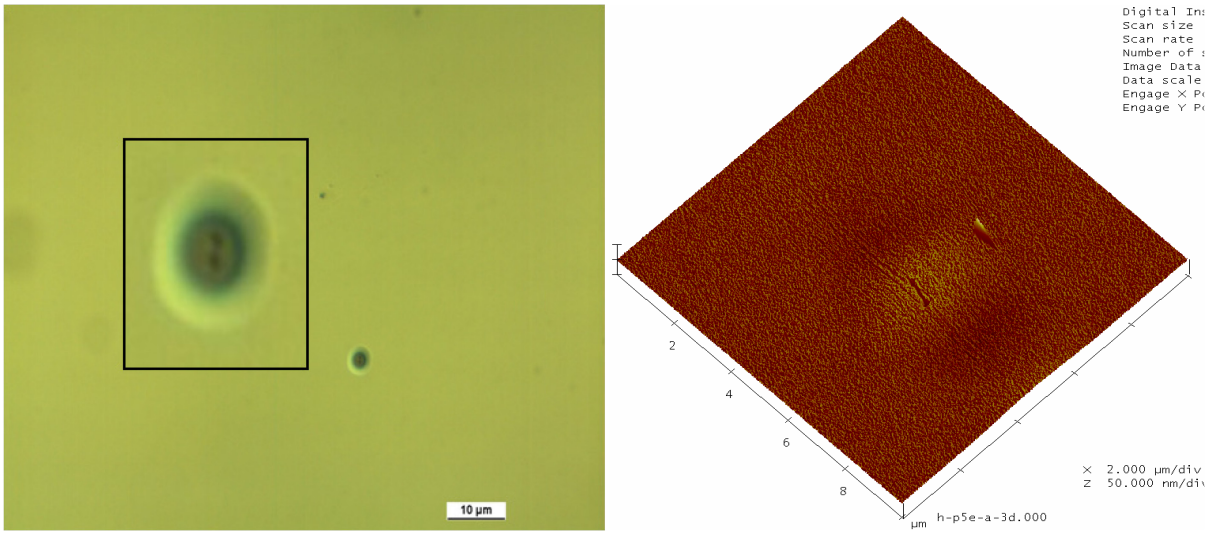


Fig. 3.54 Light optical micrograph (left, Magnified view inserted) and AFM image (right) of a 90.7 nm SOI sample, decorated with 1 ppm Cu, 800 °C; etched with dil. Secco (0.04 M Cr (VI)), dipped in HF for 45 s; residual layer thickness approx. 45 nm; OiSF visible.

Conclusion

These experiments show that the effects of copper decoration become visible at concentrations at and above 0.01 ppm of copper.

Delineation of OiSF: Chloranil etching solution compared to dilute Secco solution

The Secco etching solution contains toxic and carcinogenic chromium (Cr (VI)). One alternative solution which produced good results as a delineating agent is 2, 3, 5, 6-tetrachloro-1, 4-benzoquinone, so-called chloranil (p-CA) [113] which has a standard oxidizing potential E_0 of 712.0 mV (E_0 of $K_2Cr_2O_7$: = 1 330.0 mV).

The chloranil etching solution is composed of chloranil dissolved in dioxane with aqueous HF added to it (for details see appendix 6.1).

The etching mechanism with chloranil and HF can be described as follows:

- First the silicon is oxidized by the CA which leads to a positive charge

- The H-terminated silicon is fluorinated resulting in the formation of elemental hydrogen
- SiF_4 is formed caused by further fluorination

As the etch rate of chloranil (etching rate: 4 nm/min) is much lower than that of dilute Secco (39 nm/min.), etching times for chloranil were much longer (etching time of CA: about 14 min to etch about 55–60 nm from the initial layer thickness).

As defect densities may vary from production batch to production batch the determination of the DD of OiSF using Secco as the etching solution was repeated for the comparison with CA, whereby the wafer fragments used for both etching solutions were taken from the same batch.

The SOI-films had an initial layer thickness of 92 nm, the thickness of the BOX was 145 nm. Copper decoration was performed by furnace annealing using $Cu(NO_3)_2$ solutions in the concentrations ranging from 0.0001-10 ppm. Some of the SOI fragments were then etched with a dilute Secco (0.04 M Cr (VI)) and others with a chloranil (CA) etching solution from their initial layer thickness down to approx. 23-40 nm. After etching, the fragments were treated with a dip in HF for 45 s to delineate the defects. The defect densities obtained for all defects delineated after copper decoration (OiSF, COPs, oxygen precipitates) were compared with those of Ref 1 samples.

The average DDs are presented in Tab. 3.8. There are no data for the Ref. 2 samples and those decorated with 0.0001 ppm as the latter delaminated during the etching procedure.

The DD of Ref 1 samples etched with CA were 22x higher than those etched with dil. Secco 0.04 (M Cr (VI)). OiSF etched with CA were divided into unambiguously identified OiSF and “other” OiSF (o. OiSF). “Other” OiSF were those in which either one or both of the perforations (single or dark double dot feature) were not visible but were assumed to be OiSF because of their typical oval shape. The sum of the DD of OiSF and o. OiSF is comparable to that obtained for OiSF with Secco dil. 0.04 (M Cr (VI)). The lower oxidation potential of CA could explain its poorer etching qualities in regard to OiSFs.

After decoration with [Cu]≥ 0.01 ppm and etching using a dilute Secco the DD of the o. D. increased (DD_{mean} = 4 500–13 600 cm^{-2}). The DD of the OiSF remained in the same range (DD_{mean} = 60 700– 91 800 cm^{-2}).

The results obtained after copper decoration and etching with CA were different (Tab. 3.8):

The DD of the o. D. increased to much higher values compared to the reference sample and to the corresponding DD after using the dilute Secco. The higher the copper concentration the higher the DD of OiSF with two visible pits.

At the same time, the DD of the o. OiSF decreased with increasing copper concentration. The decoration with copper seems to magnify the pits in the OiSF due to an increase of the etch rate of the etching solution at the decorated defect caused by a reduction of the activation energy of the etching process. The crystal-lattice potential in a defect increases. These effects give rise to a higher DD of the OiSF with two visible pits.

The o.D. are mainly of COPs and oxygen precipitates, therefore the increase in their DD after copper decoration may be ascribed to enlargement of the etch pits and to the growth of oxygen precipitates.

Tab. 3.8 DD of OiSF and o. OiSF of Ref 1 and Cu decorated samples obtained after etching with CA or dilute Secco (0.04 M Cr (VI)) solution (just OiSF).

Conc. [ppm]	$\overline{DD}_{CA}[cm^{-2}]$ OiSF	$\overline{DD}_{CA}[cm^{-2}]$ o. OiSF	$\overline{DD}_{dil.Sec.}[cm^{-2}]$ OiSF
Ref 1	DD_{mean} 3 700 DD_{max} 45 400 DD_{min} 0	DD_{mean} 61 800 DD_{max} 113 400 DD_{min} 34 000	DD_{mean} 64 900 DD_{max} 113 400 DD_{min} 22 700
0.0001	DD_{mean} - DD_{max} - DD_{min} -	DD_{mean} - DD_{max} - DD_{min} -	DD_{mean} 72 600 DD_{max} 102 000 DD_{min} 22 700
0.001	DD_{mean} 12 500 DD_{max} 56 700 DD_{min} 0	DD_{mean} 28 900 DD_{max} 56 700 DD_{min} 11 300	DD_{mean} 64 600 DD_{max} 102 000 DD_{min} 22 700
0.01	DD_{mean} 11 900 DD_{max} 45 400 DD_{min} 0	DD_{mean} 24 900 DD_{max} 68 000 DD_{min} 0	DD_{mean} 67 500 DD_{max} 102 000 DD_{min} 22 700
0.1	DD_{mean} 19 300 DD_{max} 79 400 DD_{min} 0	DD_{mean} 27 200 DD_{max} 79 400 DD_{min} 0	DD_{mean} 64 100 DD_{max} 113 400 DD_{min} 34 000
1	DD_{mean} 14 700 DD_{max} 68 000 DD_{min} 0	DD_{mean} 53 300 DD_{max} 113 400 DD_{min} 22 700	DD_{mean} 91 800 DD_{max} 158 700 DD_{min} 22 700
10	DD_{mean} 38 000 DD_{max} 124 700 DD_{min} 11 300	DD_{mean} 16 400 DD_{max} 79 400 DD_{min} 0	DD_{mean} 60 700 DD_{max} 102 000 DD_{min} 22 700

In Fig. 3.55 a comparison of the DD of all OiSFs (OiSF + o. OiSF) is presented. In the reference samples the 2 perforations (dark double dots) of the OiSF pits are scarcely visible. The CA etching solution does not seem to be sensitive enough for the detection of OiSF, probably due to its lower oxidation potential compared to that of the dilute Secco etch. Copper decoration leads to a higher DD of OiSF pits with two visible perforations. The DD of OiSF pits with two visible perforations increased and that of the o. OiSF decreased with increasing copper concentration. Moreover, the higher the copper concentration the better the delineation of the OiSF with the best defect delineation of OiSF occurring at a copper concentration of 10 ppm. Copper decoration, therefore, improves the delineation of OiSF in CA-etched samples. Furthermore, very small defects such as COPs (< 20 nm) also could have been decorated and magnified due to copper silicide precipitation giving rise to further etch pits.

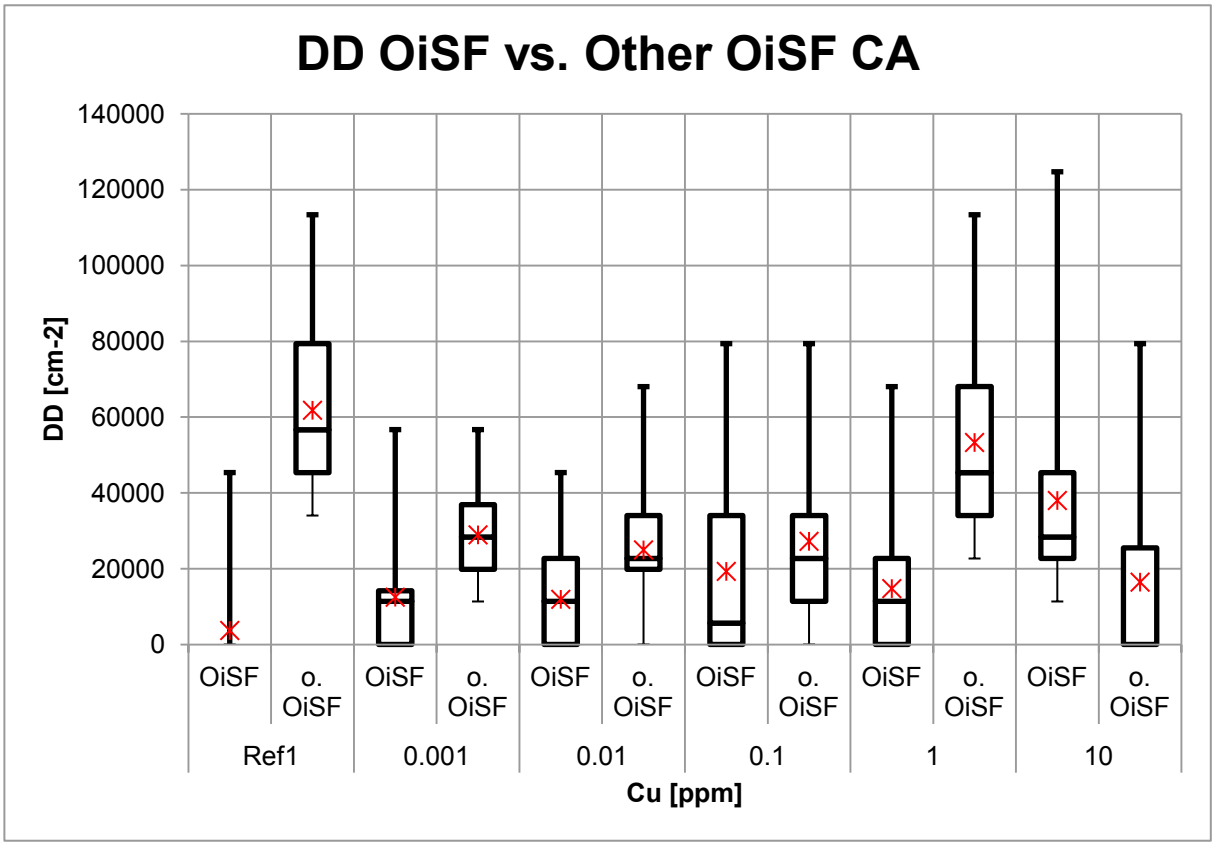


Fig. 3.55 DDs of OiSF and o. OiSF of Ref 1 and copper decorated samples etched with CA. Ref 1 (OiSF): Majority of the samples below detection limit with one outlier. 10 ppm Cu: Most samples below detection limit with few outliers.

The total DD of OiSFs (OiSF + o. OiSF) remains fairly constant after copper decoration and even with increasing copper concentration (Fig. 3.56). This supports the assumption that those etch pits with one or no typical perforation in the centre are those of OiSFs that have been poorly etched.

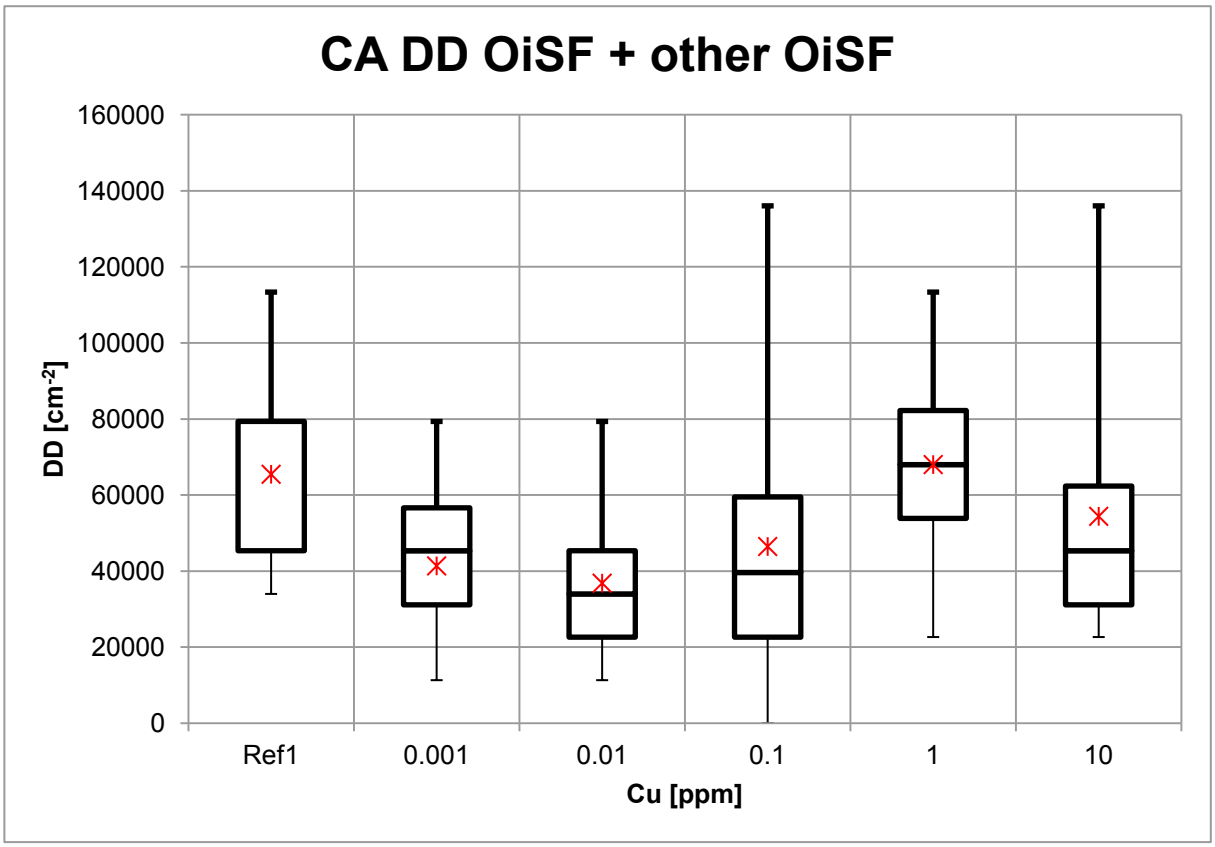


Fig. 3.56 DD of total OiSF (OiSF + o. OiSF) of copper decorated and Ref 1 samples etched with CA. Ref 1: Second quantel coincides with median.

The diagram in Fig. 3.57 shows the DD of OiSF of Ref 1 and copper decorated samples. The oxidation potential of the dilute Secco etch seemed to be high enough to reveal both perforations in all the OiSFs. The DD remains relatively constant after copper decoration regardless of the copper concentration. This result was expected because the DD of the OiSF should not increase by the decoration procedure because all OiSF are formed at the beginning of the oxidation process simultaneously. Therefore, they all have same size and there are no small OiSF which could be magnified during the annealing or the decoration step.

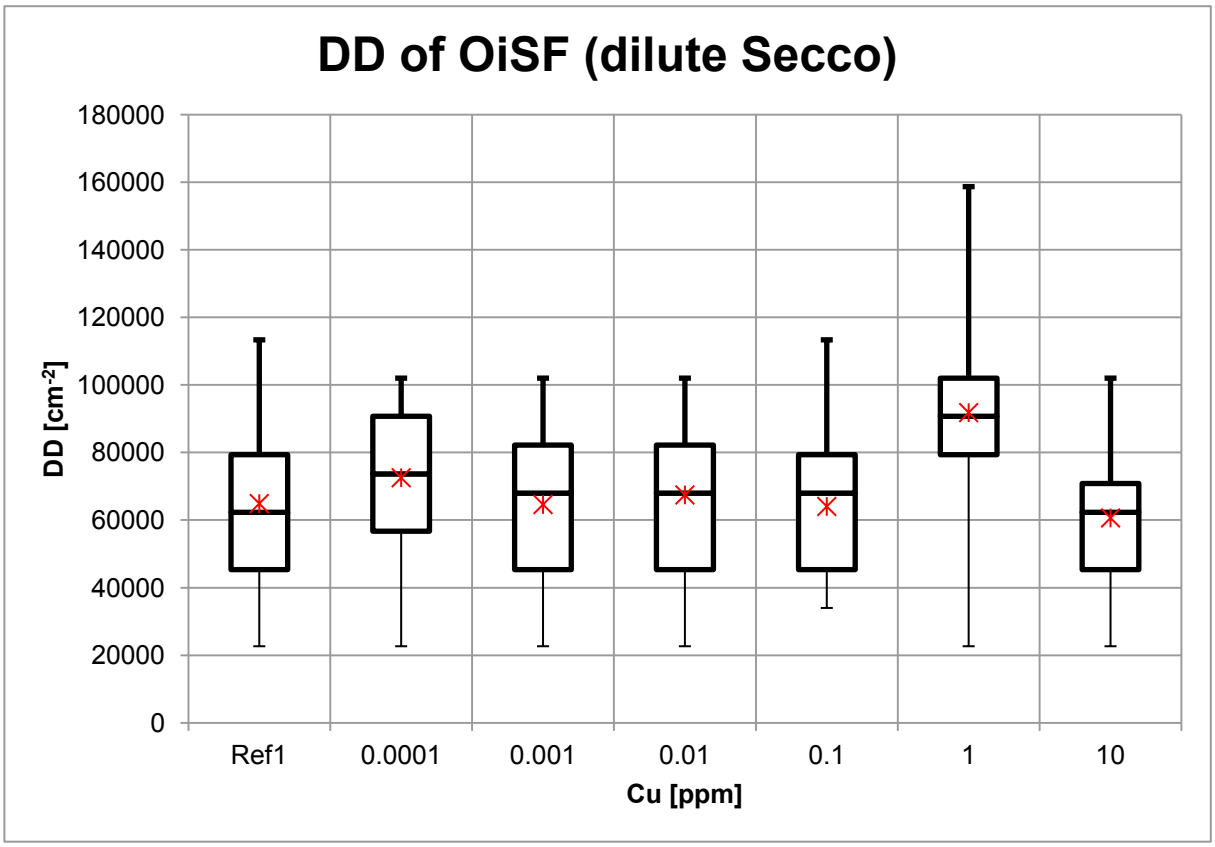


Fig. 3.57 Total DD of OiSF + o. OiSF of Ref 1 copper decorated samples etched with dil. Secco.

A comparison of DD is shown in Fig. 3.58 for Ref 1 and copper decorated samples after etching with a dilute Secco (0.04 M Cr (VI)) and a CA etch. In the case of CA the OiSF was taken as the sum of OiSF with one or no perforations and two perforations. The DD of all reference samples had nearly the same values for both etching solutions. The copper decorated samples vary in their DD being slightly higher after etching with a dilute Secco. The reason could be the higher oxidation potential of the dilute Secco.

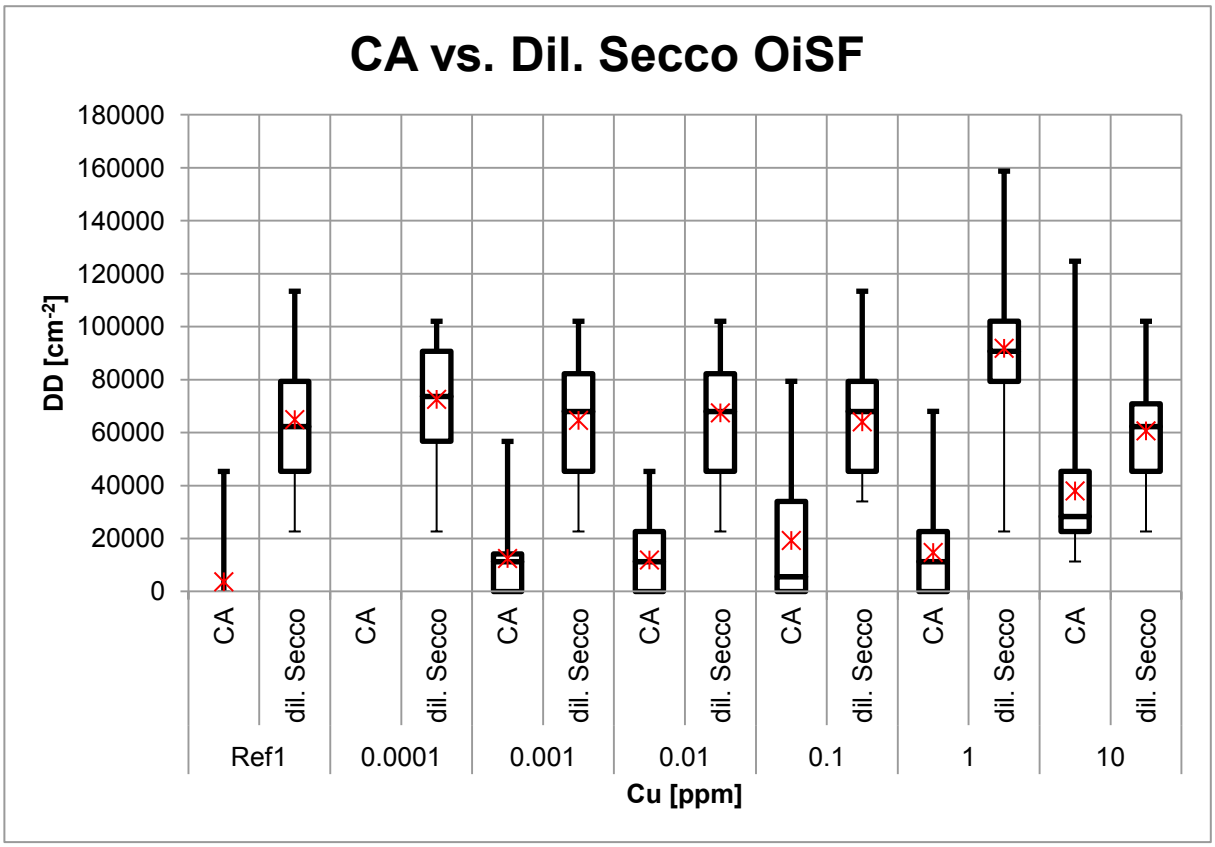


Fig. 3.58 DDs of all OiSF of Ref 1 and Cu decorated samples obtained after etching with a CA etch and with a dilute Secco (0.04 M Cr (VI)). DDs of CA-etched OiSFs are the sum of OiSFs and o. OiSFs. Ref 1 (CA): Majority of the samples below detection limit with one outlier.

Fig. 3.59 shows a light optical micrograph of a Ref 1 sample which was etched with a dilute Secco (0.04 M Cr (VI)). The OiSF pits have two visible perforations surrounded either by a bright or by a dark halo. The light optical micrographs in Fig. 3.60 and Fig. 3.61 show Ref 1 samples which were etched with a CA solution. Although the pits do not have any perforations their oval shape is typical for OiSFs.

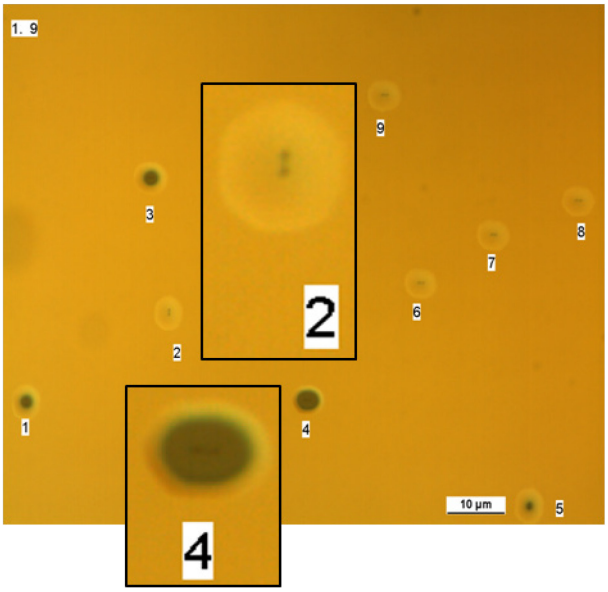


Fig. 3.59 Light optical micrograph of a 92 nm Ref 1 SOI sample; etched with dil. Secco (0.04 M Cr (VI)) dipped in HF for 45 s; residual layer thickness: approx. 34 nm, OiSF with two perforations visible. Magnified view inserted.

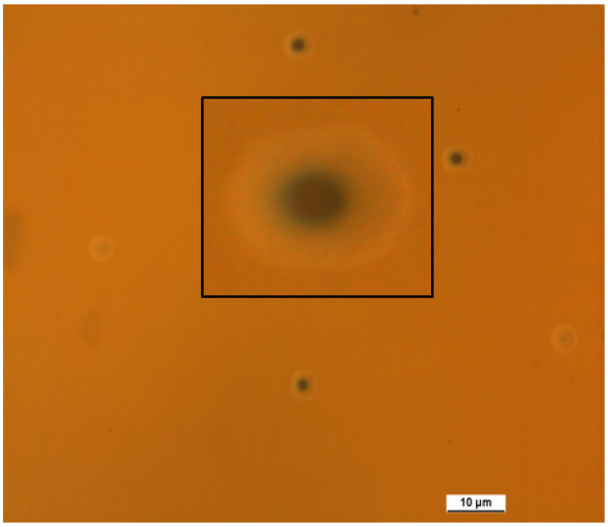


Fig. 3.60 Light optical micrograph of a 92 nm Ref 1 SOI sample etched with CA, dipped in HF for 45 s; residual layer thickness approx. 37 nm; OiSF pit without perforations. Magnified view inserted.

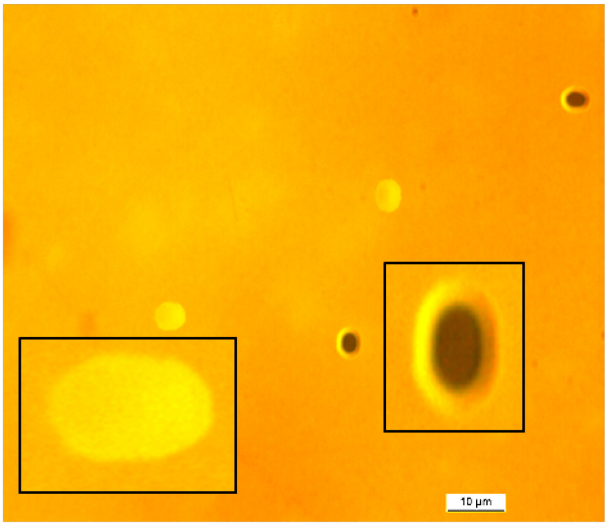


Fig. 3.61 Light optical micrograph of a 92 nm Ref 1 SOI sample etched with CA, dipped in HF for 45 s; residual layer thickness approx. 37 nm; OiSF with no perforations. Magnified view inserted.

It can be seen in Fig. 3.61 that the perforations in the pits are not visible after etching. However, halos have been formed, suggesting that the etching solution must have penetrated the surface for the HF to have reached the underlying BOX.

A light optical micrograph of a copper decorated sample (0.001 ppm Cu) which was etched with a dilute Secco is presented in Fig. 3.62. The OiSF have two visible perforations surrounded by a dark halo. The perforations are not of the same size; here we have again asymmetric etching behaviour. Fig. 3.63 shows a sample which was decorated under the same conditions but etched with a CA solution. The OiSF have their typical oval shape and although the perforations are absent, the shape of the pits indicate that they are OiSFs.

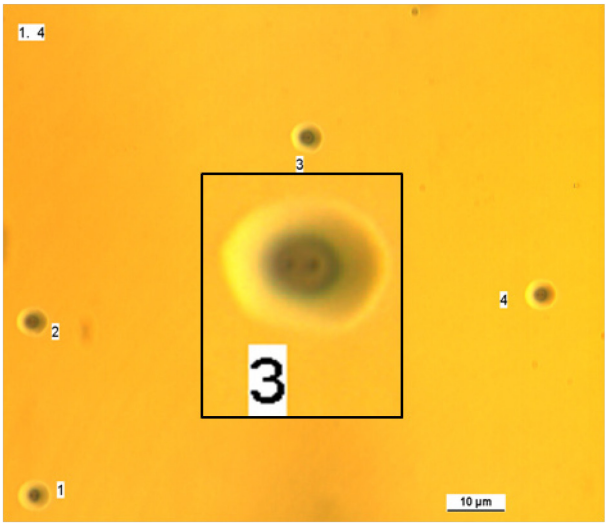


Fig. 3.62 Light optical micrograph of a 92 nm SOI sample decorated with 0.001 ppm copper, annealed at 800 °C, etched with dil. Secco (0.04 M Cr (VI)), dipped in HF for 45 s; residual layer thickness approx. 34 nm. OiSF with two pits. Magnified view inserted.

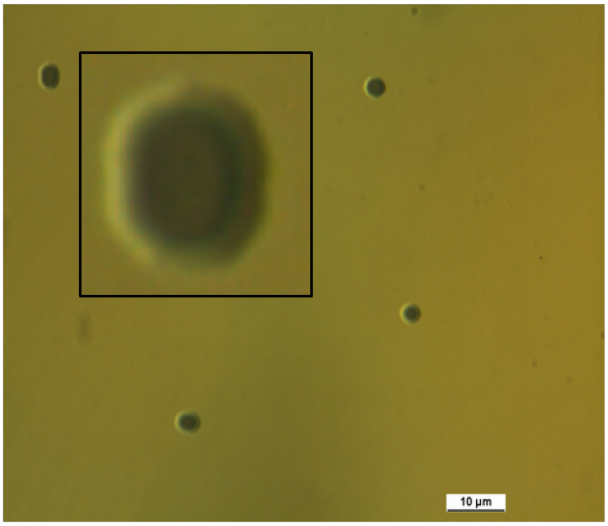


Fig. 3.63 Light optical micrograph of a 92 nm SOI sample decorated with 0.001 ppm, annealed at 800 °C; etched with CA, dipped in HF for 45 s; residual layer thickness approx. 37 nm. OiSF with no pits. Magnified view inserted.

With 0.01 ppm Cu both DD and appearance of the OiSF pits showed little or no difference to those obtained with 0.001 ppm Cu.

Some samples were investigated in more detail via a SEM. Fig. 3.64 shows a light optical micrograph (left) and a SEM image (right) of the same sample. The fragment was decorated with 0.1 ppm of copper and etched with a dilute Secco.

Each of the images shows one OiSF pit with two perforations. In the SEM image the connecting “line” – the stacking fault – is visible. In the light optical micrograph a pale oval “cloud” can be seen around the OiSF that slants down to a dark area in the centre surrounding the perforations which is the SOI layer that has sunk to the substrate and therefore appears dark in the light optical micrograph. OiSF pits with dark centers appeared more frequently in copper decorated samples than in undecorated ones as the etch rate is higher at the copper silicide in the defect.

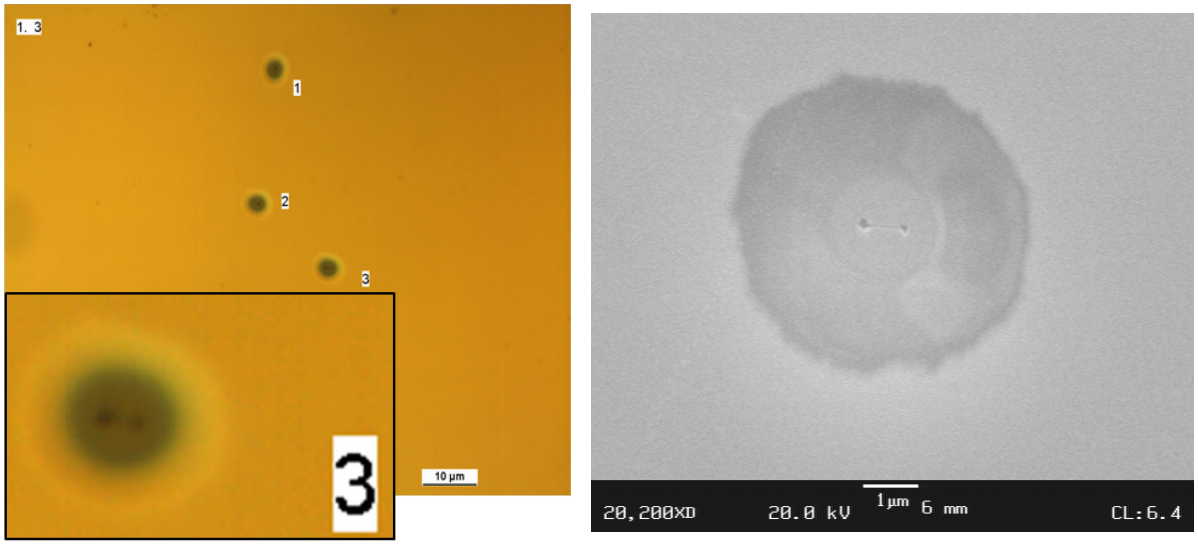


Fig. 3.64 Light optical micrograph (left, magnified view inserted) and SEM (right) of a 92 nm SOI sample decorated with 0.1 ppm, annealed at 800 °C, etched with dil. Secco (0.04 M Cr (VI)); dipped in HF dip for 45 s; residual layer thickness approx. 34 nm OiSF with two pits.

Fig. 3.65 presents a light optical micrograph (left) and a SEM image (right) of the same sample. The fragment was decorated with 0.1 ppm of copper and etched with a CA solution.

The results shown in Fig. 3.65 suggest that the concentration of copper has to be at least 0.1 ppm for a delineation of OiSFs with CA comparable to that of dil. Secco (0.04 M Cr (VI)). In a redox process, copper appears to increase the sensitivity of the etching solution. In the light optical micrograph, the upper magnified image shows the 2 perforations surrounded by a “cloud” which speaks for an intact SOI layer around the OiSF after the dip in HF. On the other hand the lower image shows a pit where the dark SOI layer surrounding the OiSF has definitely sunk to the substrate. In the SEM image (right) the upper OiSF appears as an oval cloud where the paler area passes gently into the darker area which seems to have sunk around the stacking fault. The lower pit however, appears deeper and the core area seems to have sunk to the bottom. The sloping edge provides the contrast. There is only a hint of the stacking fault line, in contrast to OiSFs etched with Secco (0.04 M Cr (VI)) where they are plainly visible.

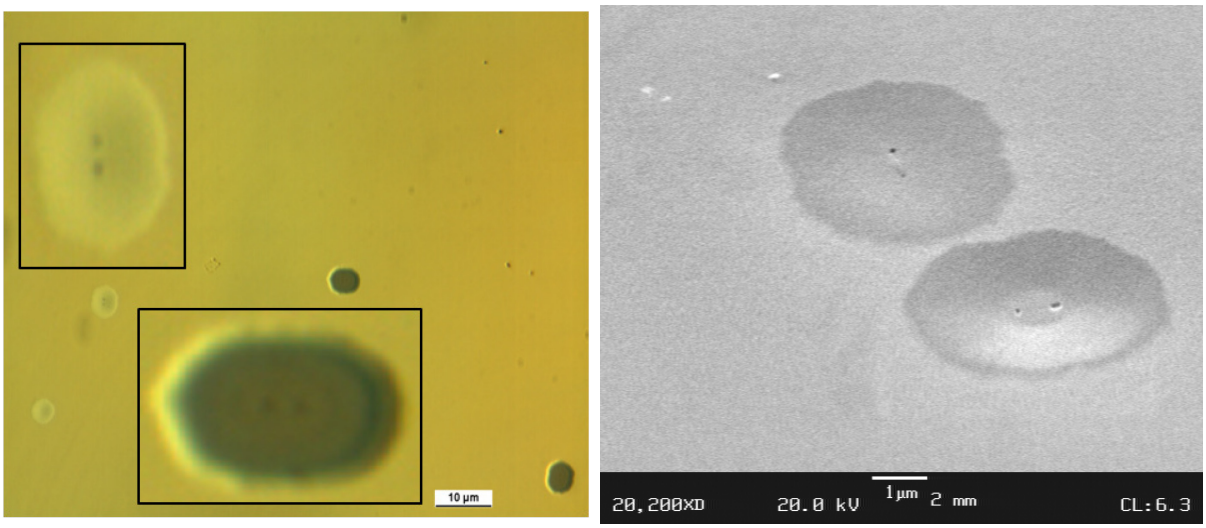


Fig. 3.65 Light optical micrograph (left, magnified view inserted) and SEM (right) of a 92 nm SOI sample decorated with 0.1 ppm, annealed at 800 °C, etched with CA, dipped in HF for 45 s; residual layer thickness: approx. 38 nm; OiSF with two pits.

SOI samples were decorated with 1 ppm of copper and etched with a dilute Secco (0.04 M Cr (VI)) (Fig. 3.66). The OiSF pits have two visible perforations surrounded mainly by a dark halo in contrast to the samples which were copper decorated (1 ppm Cu) and etched with a CA etch (Fig. 3.67). The defects are typically oval with just one or no perforation in the pit similar to those in the reference samples.

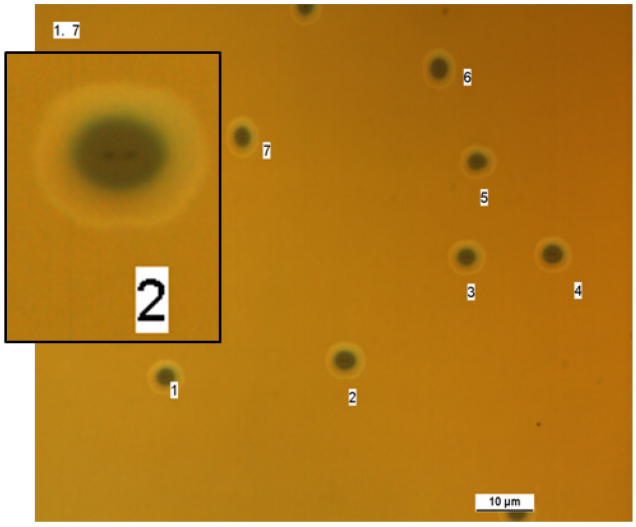


Fig. 3.66 Light optical micrograph of a 92 nm SOI sample decorated with 1 ppm Cu, annealed at 800 °C, etched with dil. Secco (0.04 M Cr (VI)), dipped in HF for 45 s; residual layer thickness approx. 38 nm; OiSF visible. Magnified view inserted.

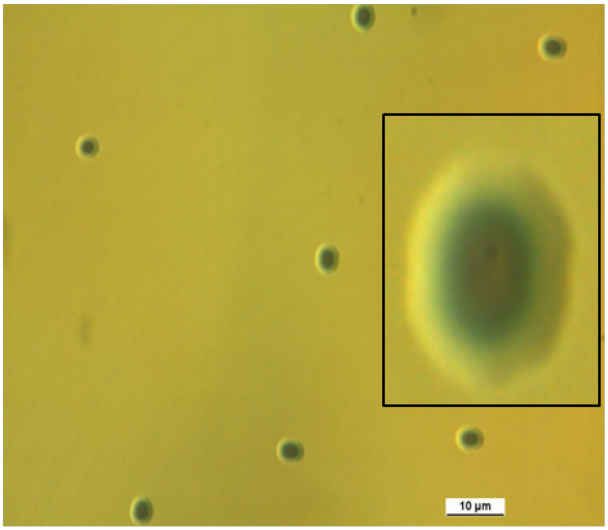


Fig. 3.67 Light optical micrograph of a 92 nm SOI sample decorated with 1 ppm, annealed at 800 °C, etched with CA, dipped in HF for 45 s; residual layer thickness approx. 37 nm; OiSF with one or no pit. Magnified view inserted.

The highest DD of OiSF having two visible perforations after etching with a CA etchant was obtained using concentrations of [Cu] = 10 ppm. Therefore, a copper concentration of [Cu] = 10 ppm seems to increase the etch rate of the etching solution at the decorated partial dislocation of the OiSF due to a reduction of the activation energy of the etching process and an increase of the crystal-lattice potential at the defect which leads to the delineation of most both pits in the OiSF.

Conclusion

Copper decoration at and above 0.01 ppm improves the detection of OiSF etched with a CA solution, but does not attain the efficiency of dil. Secco (0.04 M Cr (VI)) which has a higher oxidizing potential.

3.8 Copper decoration of crystal defects in thick SOI

Copper decoration combined with preferential etching studies were performed on 610 nm and 1 400 nm thick SOI films for the development of a procedure for copper decoration of crystal defects in thick SOI samples. The BOX thickness was about 300 nm for the 610 nm and about 1 000 nm for the 1 400 nm SOI wafer.

Two types of defects could be delineated in thick SOI (Fig. 3.68):

- *Defects with a halo*

  These defects may originate from the upper part of the SOI film. They give rise to etch pits which protrude down to the BOX. The halo is produced during the dip in HF which etches the BOX below the etch pits.

  The average radii of these pits were 2.4 µm without copper decoration and 3.2-5.1 µm after copper decoration using dil. Secco (0.04 M Cr (VI)).

- *Defects without a halo*

  These defects may lie in the deeper parts of the SOI film producing etch pits which do not reach the underlying BOX. The box is consequently not etched by HF.

  The average radii of these etch pits were 0.4 µm without copper decoration and 0.5-0.6 µm after copper decoration using dil. Secco (0.04 M Cr (VI)).

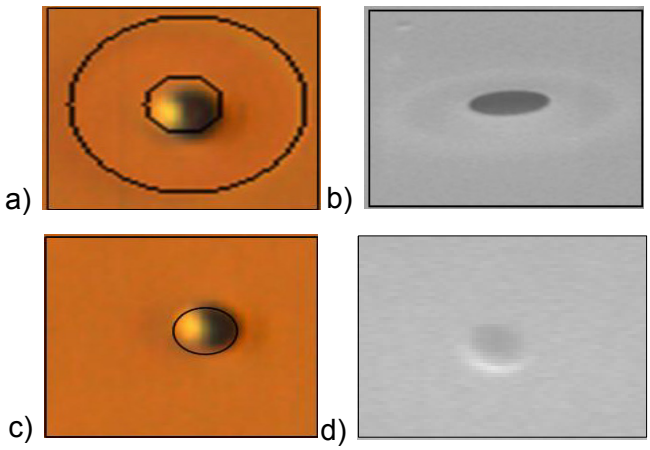


Fig. 3.68 Light optical micrographs (a + c) and SEM (b + d) of defect with a halo (a + b) and defects without a halo (c + d).

3.8.1 1 400 nm thick SOI

SOI wafers with a silicon film thickness of 1 400 nm and a BOX thickness of 1 000 nm (“thick SOI”) were cut into fragments. Three different preferential etching solutions were used for the delineation of crystal defects with and without copper decoration.

The experimental conditions like Cu concentration and annealing temperature in the furnace used for copper decoration studies were developed and optimized in regard to the diffusion of copper through the thick BOX layer (1 000 nm).

The optimal annealing temperature for the copper decoration procedure was determined first. The BOX layer in standard SOI is 145 nm thick. The copper deposited on the back of the fragment easily penetrates this layer at 800 °C. However, the 1 000 nm thick BOX layer in the thick SOI acts as a strong diffusion barrier for copper. However, at 950 °C sufficient copper diffuses through the BOX into the SOI layer and decoration of the defects occurs [114].

Copper decoration was carried out as described in the foregoing experiments but with the fragments being annealed at 950 °C instead of 800 °C for 1 min. This was followed by etching the SOI layer down to a thickness of about 50 nm with different preferential etchants.

As the Secco etching solution contains toxic and carcinogenic chromium (Cr (VI)) two alternative solutions which produced good results especially with thick SOI because of their higher etching rates were also tested. Their standard oxidizing potentials E_0 are considerably lower than that of the dil. Secco (0.04 M Cr (VI)) (see Tab. 3.9). Detailed information about etchants used is given in the appendix.

Tab. 3.9 Composition and properties of etching solutions used.

Etching solution	Composition	Etch rate [nm/s]	Oxidizing potential E_0 [mV]
Dil. Secco (0.04 M Cr (VI))	$K_2Cr_2O_7$ HF H_2O	0.6 - 0.7	1 330
Jeita A	HNO_3 HF HAc, H_2O	4.5	960
Jeita B	HNO_3 KI HF HAc, H_2O	5.7	960

A dip in HF for approx. 90 s served to etch the buried oxide below the pits thus producing a halo under an optical light microscope. Selected defects were analyzed with a scanning electron microscope (SEM). After copper decoration and subsequent preferential etching with the three etching solutions mentioned earlier the defect densities were determined for defects with and without a halo.

There are no data for the Ref 2 samples.

Copper decoration with preferential etching using dil. Secco 0.04 M Cr (VI)

The etching duration was 34 min 30 s with an etch rate of 0.6-0.7 nm/s for the fragment etched with dilute Secco (0.04 M Cr (VI)).

Fig. 3.69 shows a light optical micrograph of a non-decorated and non-annealed Ref 1 sample with two types of etch features corresponding to defects:

- Pits surrounded by a halo (“1”)
- Pits without a halo (“2”)

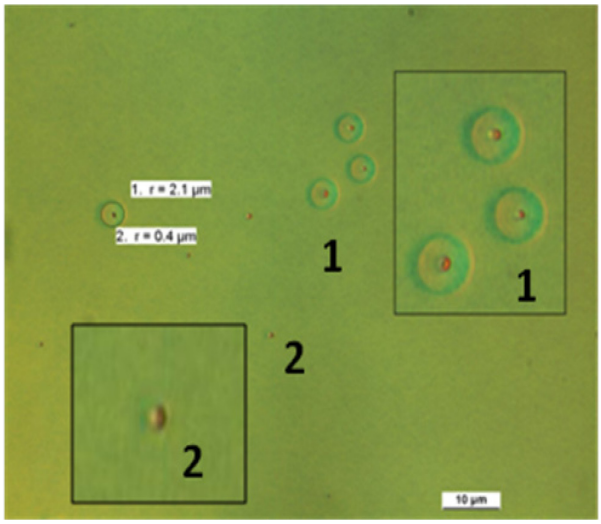


Fig. 3.69 Light optical micrograph of a 1 400 nm thick SOI reference sample etched with dil. Secco (0.04 M Cr (VI)) and dipped in HF for 45 s; residual layer thickness: approx. 50 nm. Magnified view in inserts. Pits with halo ("1") and pits without halo ("2") are displayed.

Fig. 3.70 displays a light optical micrograph and a SEM image of a thick SOI fragment decorated with 1 ppm copper and etched with dil. Secco. A few pits with halos and a high number without halos are visible. Both pits and halos are larger than those of the non-decorated thick SOI fragments. This is caused by the higher etch rate at the copper silicide precipitates at the defects. The SEM micrograph clearly reveals pits of different sizes (dark contrast) and halos (bright rings around pits indicate their extension).

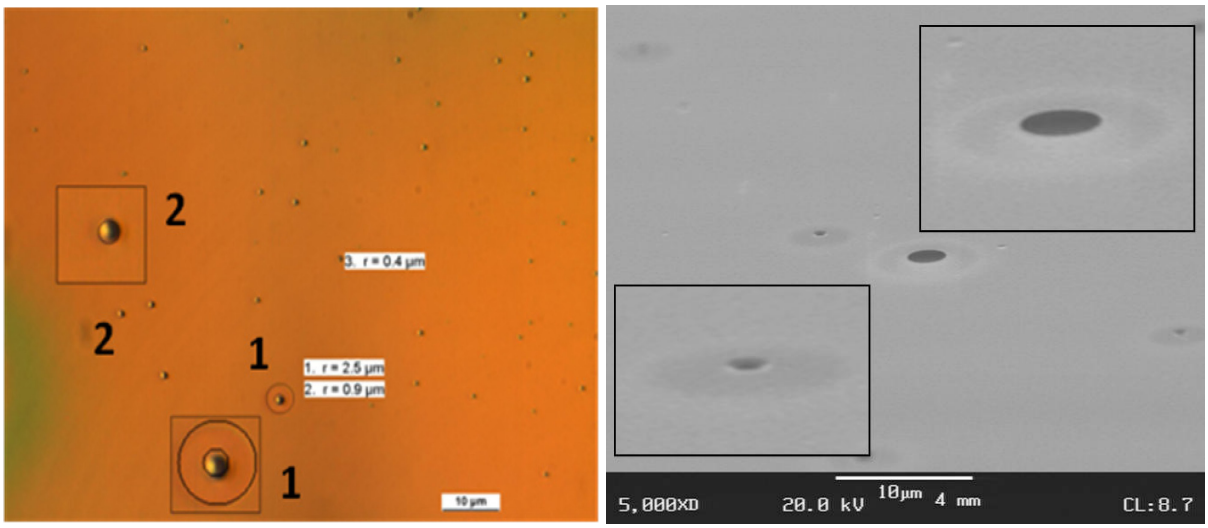
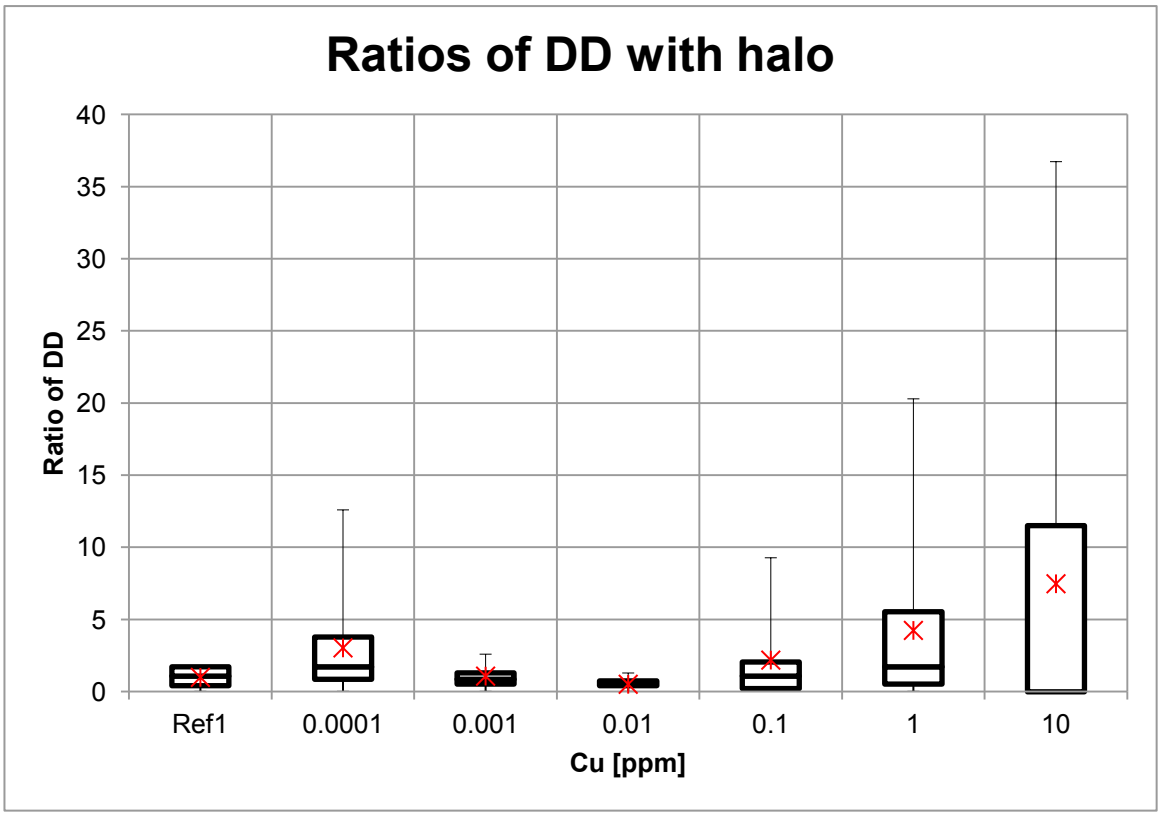


Fig. 3.70 Light optical micrograph (left) and a SEM image (right) of a 1 400 nm thick SOI sample decorated with 1 ppm copper, annealed at 950 °C, etched with dil. Secco (0.04 M Cr (VI)) and dipped in HF for 90 s; residual layer thickness: approx. 50 nm. Defects (pits) with a halo ("1") and without a halo ("2") are visible. Magnified view in insert. In a) at some magnified defects a circle was drawn to determine the pit radius.

Fig. 3.71 shows the ratios of the DD of Ref 1 and copper decorated fragments separated into defects with a halo (Fig. 3.71a) and defects without a halo (Fig. 3.71b). In both diagrams the DD of the Ref 1 are comparable to those of fragments decorated with a low copper concentration. The DD increase significantly for both etch pit types at and above a copper concentration of 0.1 ppm and may be ascribed to copper decoration. The reason for the high DD at a Cu concentration of 0.0001 ppm in the figure a) is not known. A copper concentration of 10 ppm resulted in much higher DD. On the one hand this may be attributed to small defects made visible by copper decoration which would not have been revealed by etching alone. On the other hand copper precipitation induced artefacts could also have contributed to the high defect densities obtained.

a)



b)

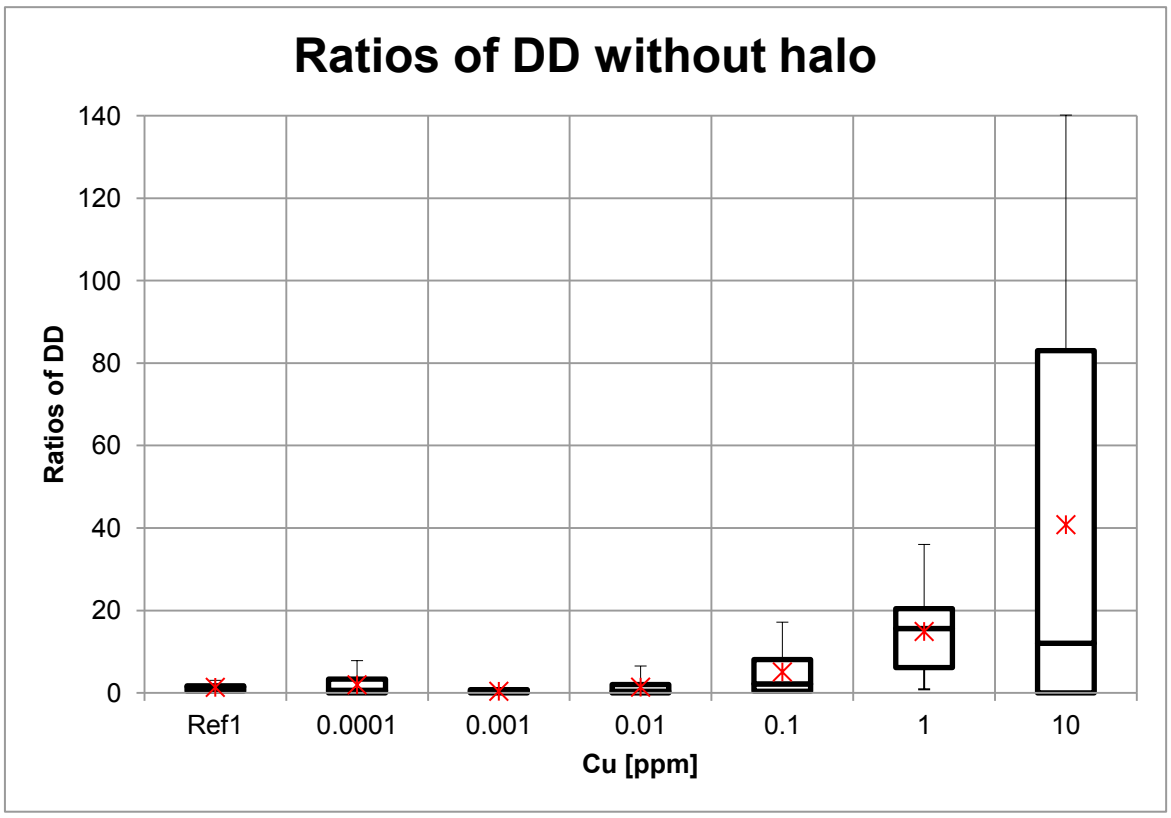
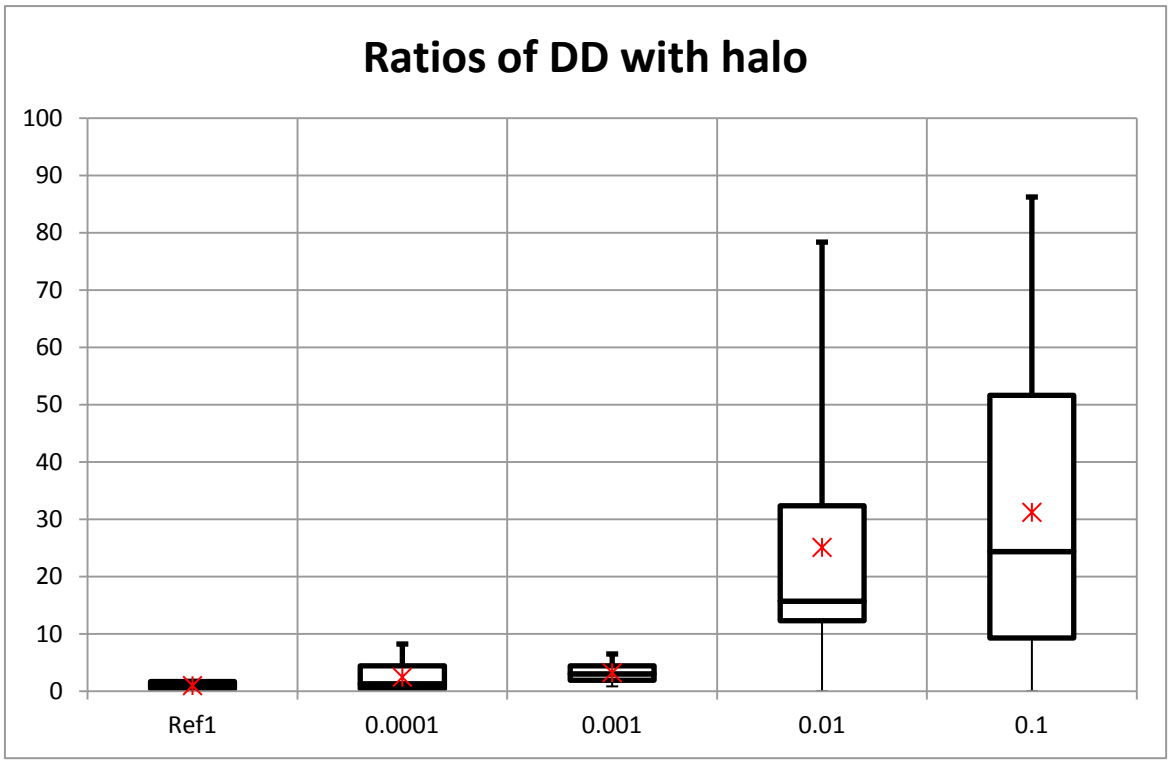


Fig. 3.71 Ratios of defect densities of etch pits with halos (a) and without halos (b) on 1 400 nm thick SOI decorated with copper, annealed at 950 °C etched with dil. Secco (0.04 M Cr (VI)). The DD are normalized to the value of the dil. Secco Ref 1 with halo.
Ref 1 in a): Second quantel coincides with median.

Fig. 3.72 shows the results of a closer examination of copper decoration with concentrations of copper ranging from 0.0001 to 0.1 ppm to determine at which copper level enhanced copper decoration of defects occurs. Again the DD obtained of defects with a halo (Fig. 3.72a) and without a halo (Fig. 3.72b) are compared. The data show a distinctly increased DD for both types of etch pits at and above a copper concentration of 0.01 ppm.

a)



b)

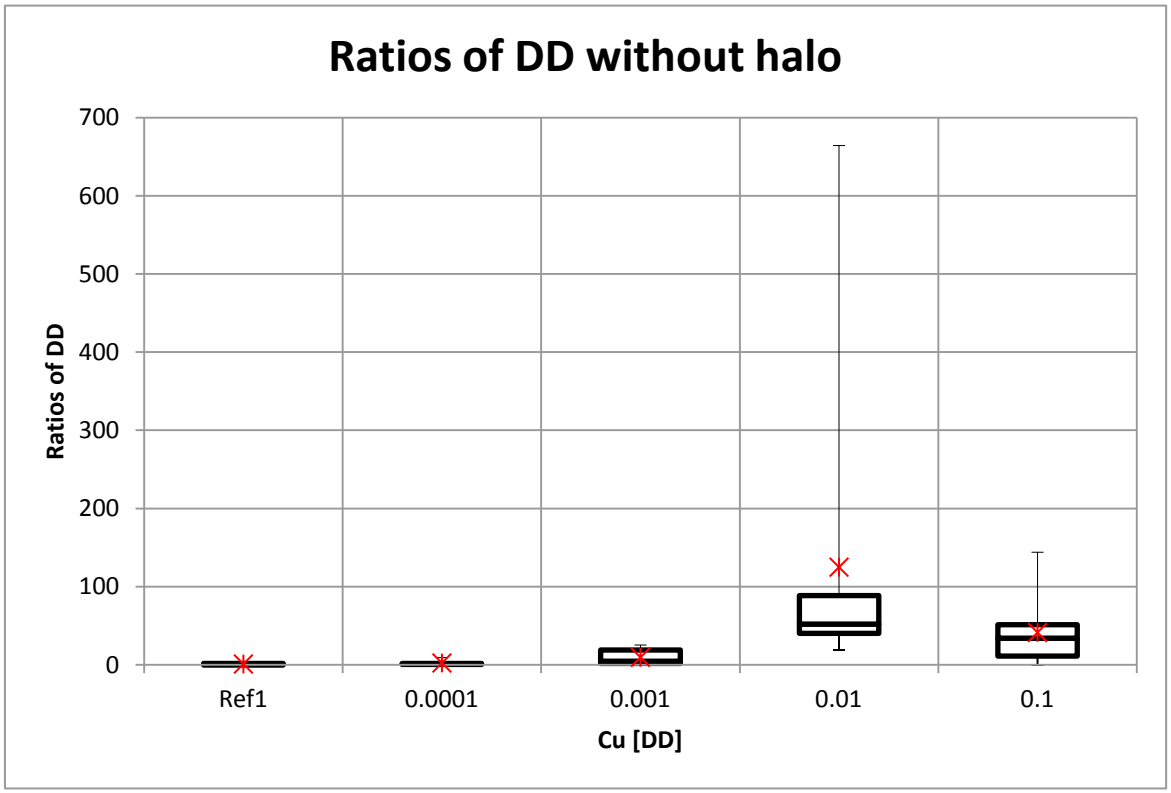


Fig. 3.72 Ratios of the defect densities (DD) determined by dil. Secco etch (0.04 M Cr (VI)): Densities of pits a) with a halo and b) without a halo are plotted for thick SOI decorated with 0.0001-0.1 ppm Cu and annealed at 950 °C. The DD are normalized to the value of the dil. Secco Ref 1 with halo.

These results indicate that copper concentrations around 0.01 to 0.1 ppm provide suitable decoration conditions for defects in thick SOI and are a threshold beyond which defects not

revealed without decoration are clearly delineated after copper decoration by a dilute Secco etch. Although the true nature of the defects cannot be deduced from the etch pits it is very likely that the increase in density of pits revealed via copper decoration are attributable to small oxygen precipitates (“oxygen nuclei”) and small COPs.

Copper decoration with preferential etching using Jeita B (with potassium iodide)

Thick SOI fragments were etched with a Jeita B etchant [115] (Tab. 3.9) after copper decoration using concentrations ranging from 0.0001-10 ppm of Cu in a $Cu(NO_3)_2$ solution followed by furnace annealing at 950 °C.

The etching duration was 4 min 30 s with an etching rate of 5.7 nm/s.

Fig. 3.73 shows a non-decorated Ref 1 sample etched with Jeita B while Fig. 3.74 is an image of a sample decorated with 0.1 ppm copper. Defects with halos, “1” in Fig. 3.74 and without halos, “2” in the Fig. 3.73 and Fig. 3.74 are visible.

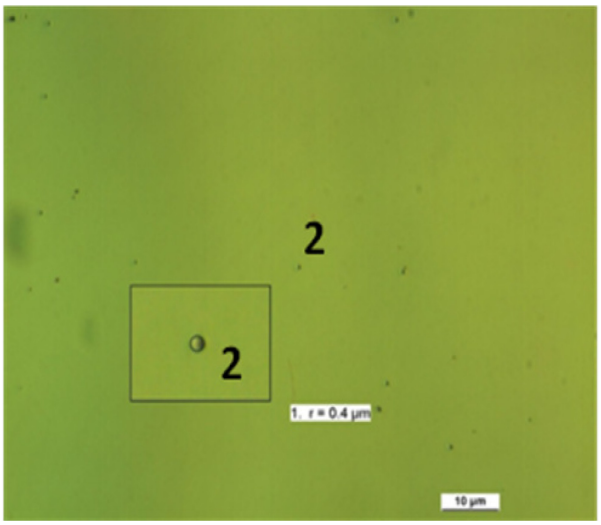


Fig. 3.73 Light optical micrograph of a 1 400 nm thick SOI Ref 1 fragment etched with Jeita B dipped in HF for 90 s; remaining layer thickness: approx. 50 nm. Magnified view in insert. At some magnified defects a circle was drawn to determine the pit radius.

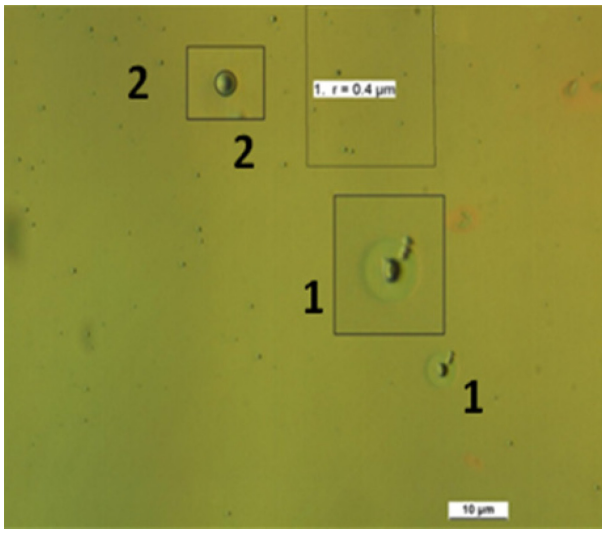
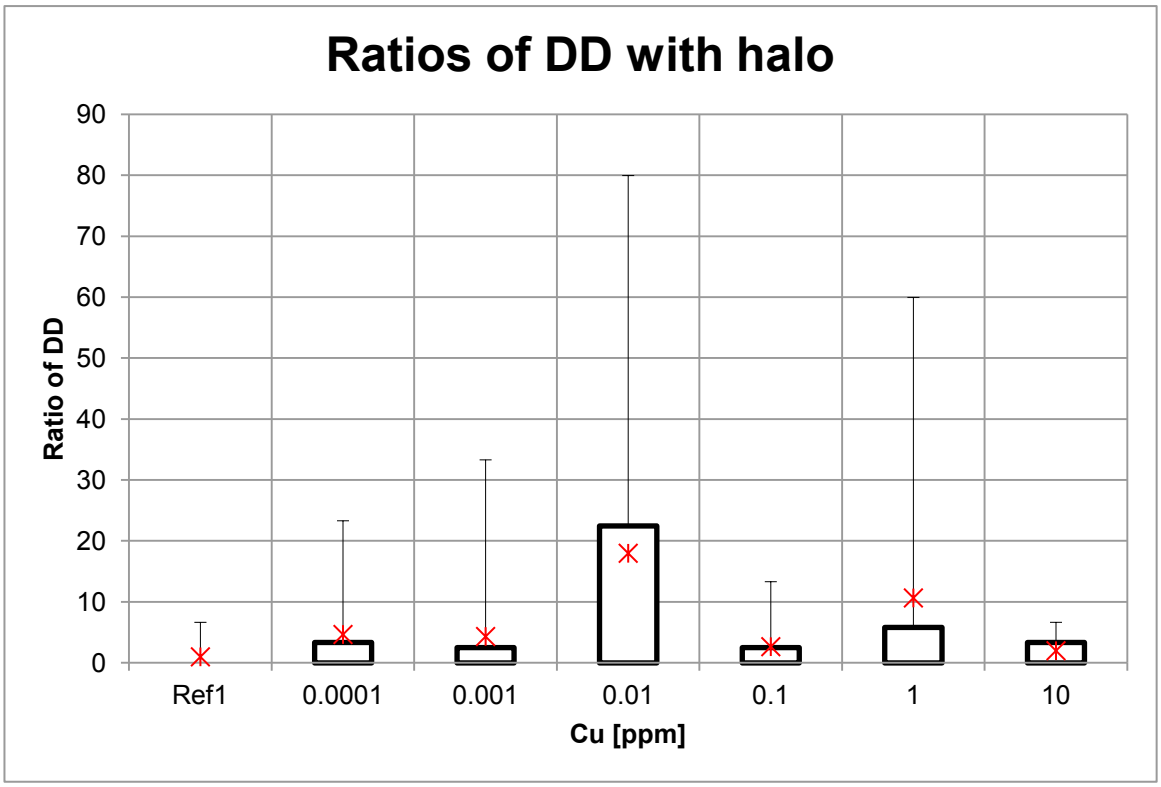


Fig. 3.74 Light optical micrograph of a 1 400 nm thick SOI sample decorated with 0.1 ppm copper, annealed at 950 °C, etched with Jeita B and dipped in HF for 90 s; residual layer thickness: approx. 50 nm. Magnified view in insert. At some magnified defects a circle was drawn to determine the pit radius.

Fig. 3.75 shows the ratio of the defect densities of Ref 1 and copper decorated fragments separated into defects with a halo (Fig. 3.75a) and defects without a halo (Fig. 3.75b). No clear relationship can be seen between copper concentration and the ratios of defect densities. The densities of defects without a halo determined by Jeita B are more than one order of magnitude higher than those obtained after etching with Secco (0.04 M Cr (VI)). This may be the result of the considerably lower oxidizing potential of the Jeita B etchant compared to that of the dil. Secco (0.04 M Cr (VI)). Furthermore, the selectivity S of the Jeita etching solutions is with a value of 1.5 much lower than that of the dilute Secco (S = 2.4) [116]. An etching solution with a higher selectivity leads to deeper etch pits. That is why the Jeita etchant produces small and shallow etch pits in general. Therefore, it can be inferred that most of the pits do not protrude down to the BOX after etching with Jeita B, hence, they result in a much lower DD of defects with a halo.

An increased formation of copper induced artefacts caused by the presence of the KI in the Jeita solution due to an electrochemical interaction between copper, silicon and KI can be ruled out. Artefact formation should occur at the sample surface. However, after etching they should lead to etch pits which protrude down to the BOX and produce a halo.

a)



b)

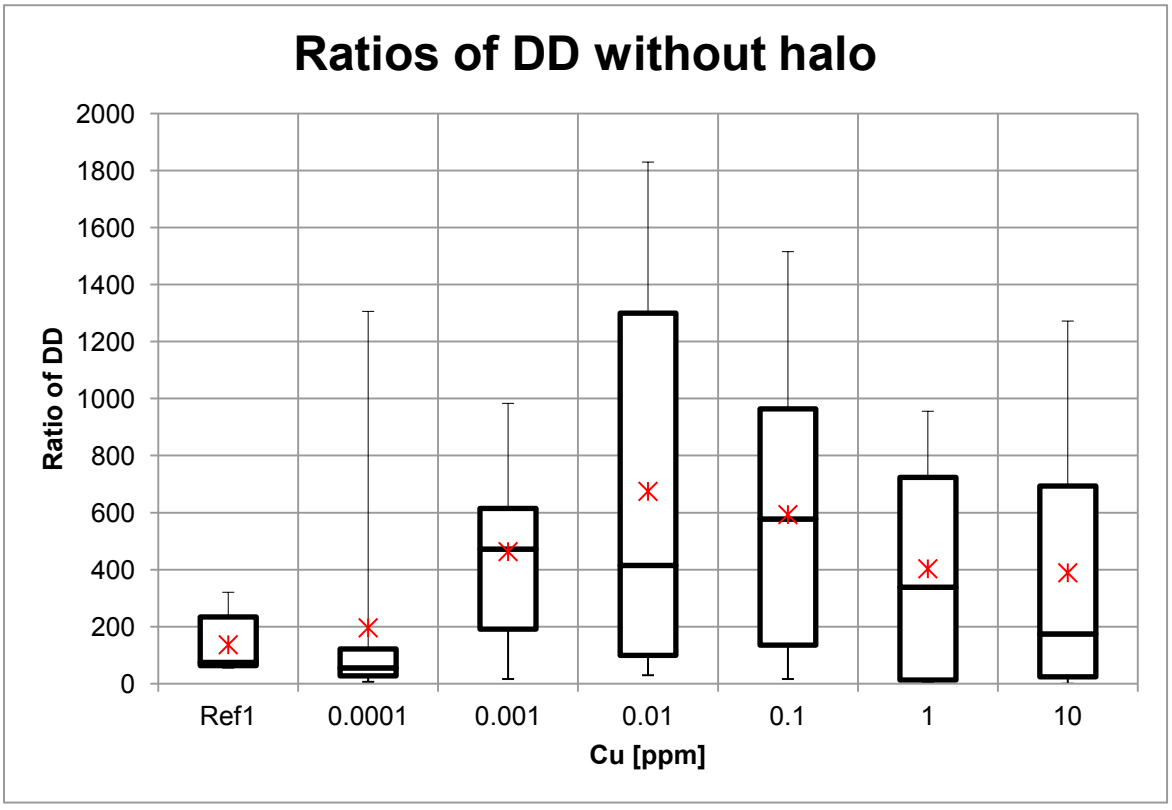


Fig. 3.75 Ratios of densities of defects a) with a halo and b) without a halo on thick SOI etched with Jeita B, decorated with 0.0001–10 ppm Cu, annealed at 950°C. The DD are normalized to the value of the Jeita B Ref 1 with halo.
Ref 1 in a): Majority of the samples below detection limit with one outlier. 0.0001-10 ppm Cu in a): Sharp distribution close to detection limit.

Copper decoration with preferential etching using Jeita A

Jeita A [115] (Tab. 3.9) is similar to Jeita B in composition but does not contain potassium iodide.

Thick SOI samples were etched with a Jeita A etchant after copper decoration using concentrations ranging from 0.0001-10 ppm of Cu in a $Cu(NO_3)_2$ solution followed by furnace annealing at 950 °C.

The etching duration was 5 min with an etch rate of 4.5 nm/s.

Fig. 3.76 presents an image of a Ref 1 sample without prior treatment preferentially etched with Jeita A. The defects detected were without halos.

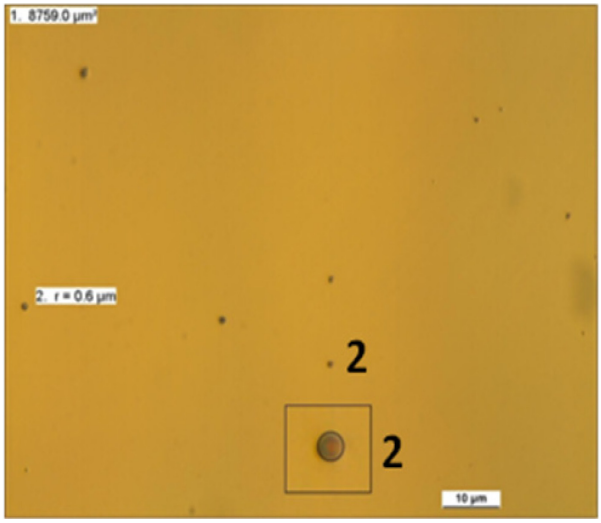


Fig. 3.76 A light optical micrograph of a 1 400 nm thick SOI Ref 1 sample etched with Jeita A and dipped in HF for f90 s; residual layer thickness: approx. 50 nm. Defects (pits) without a halo ("2") but none with a halo are visible. Magnified view in insert. At some magnified defects a circle was drawn for determination of the pit radius.

A thick SOI fragment decorated with 0.1 ppm copper is displayed in Fig. 3.77. In contrast to the reference fragment both defects with halos "1" and defects without halos "2" were found.

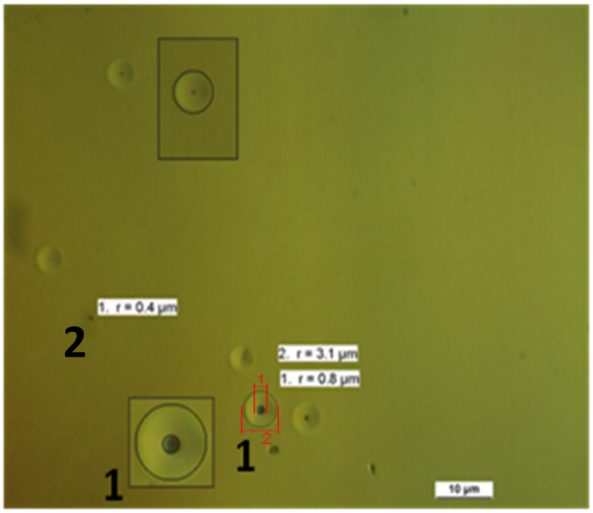
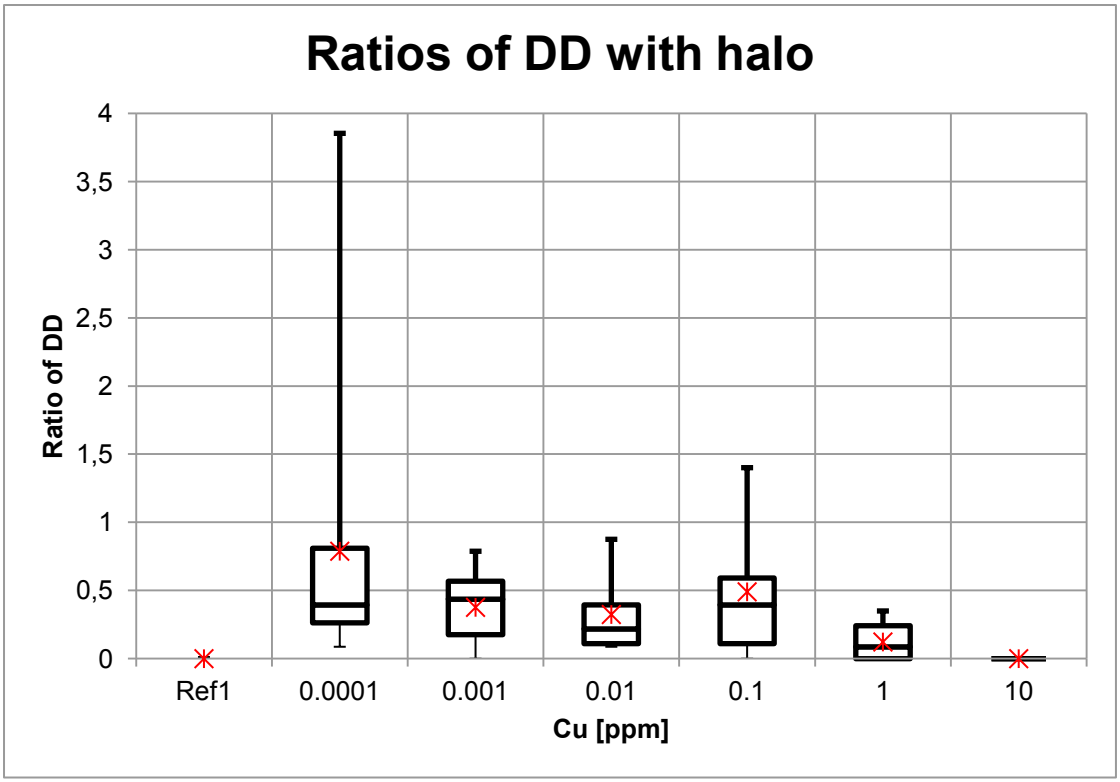


Fig. 3.77 Light optical micrograph of a 1 400 nm thick SOI sample decorated with 0.1 ppm copper, annealed at 950 °C, etched with Jeita A and dipped in HF for 90 s; residual layer thickness: approx. 50 nm. Defects (pits) with a halo ("1") are visible. Magnified view in inserts. At some magnified defects a circle was drawn to determine the pit radius.

Defect densities with and without a halo are shown and compared in Fig. 3.78. There were no pits with halos in the reference sample. After copper decoration defects with a halo could be detected. Copper increases the etch rate at the defect which leads to the formation of some etch pits with halos. Again no clear relationship was found between copper concentration and increase in defect densities obtained. At a copper concentration of 10 ppm etching with Jeita A produced densities of defects without a halo that were about one order of magnitude higher than those at the lower copper levels. At this high copper concentration the formation of copper induced artefacts at the surface cannot be ruled out.

a)



b)

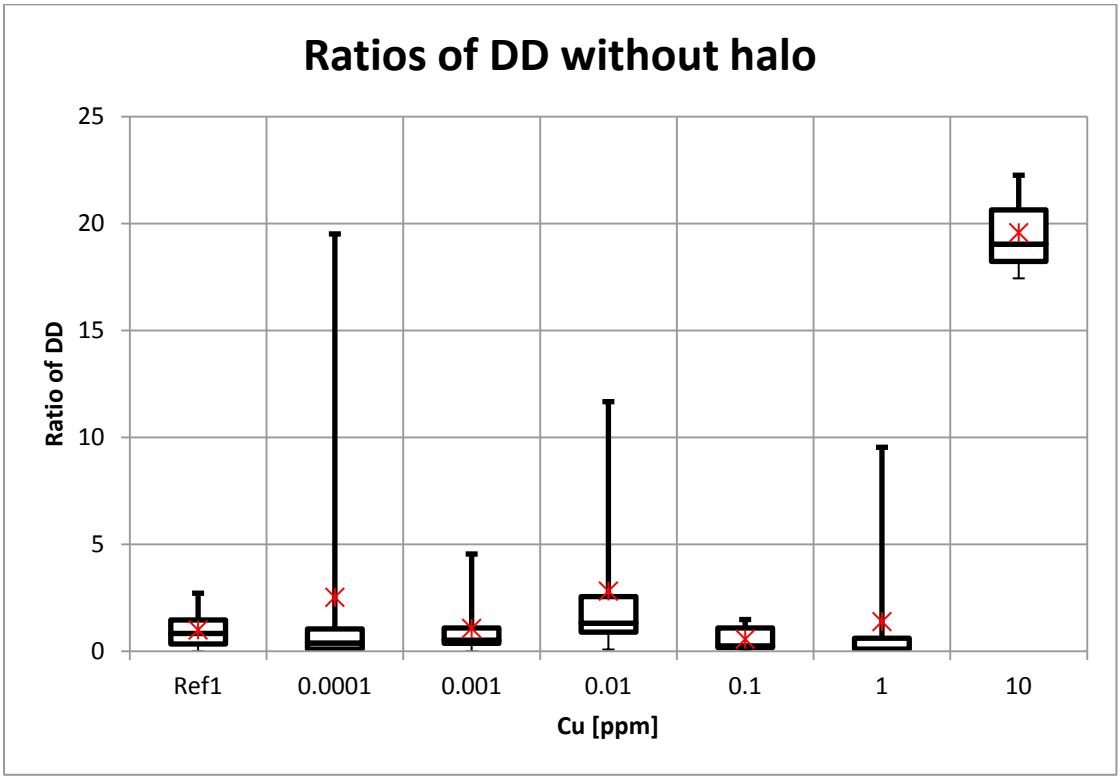
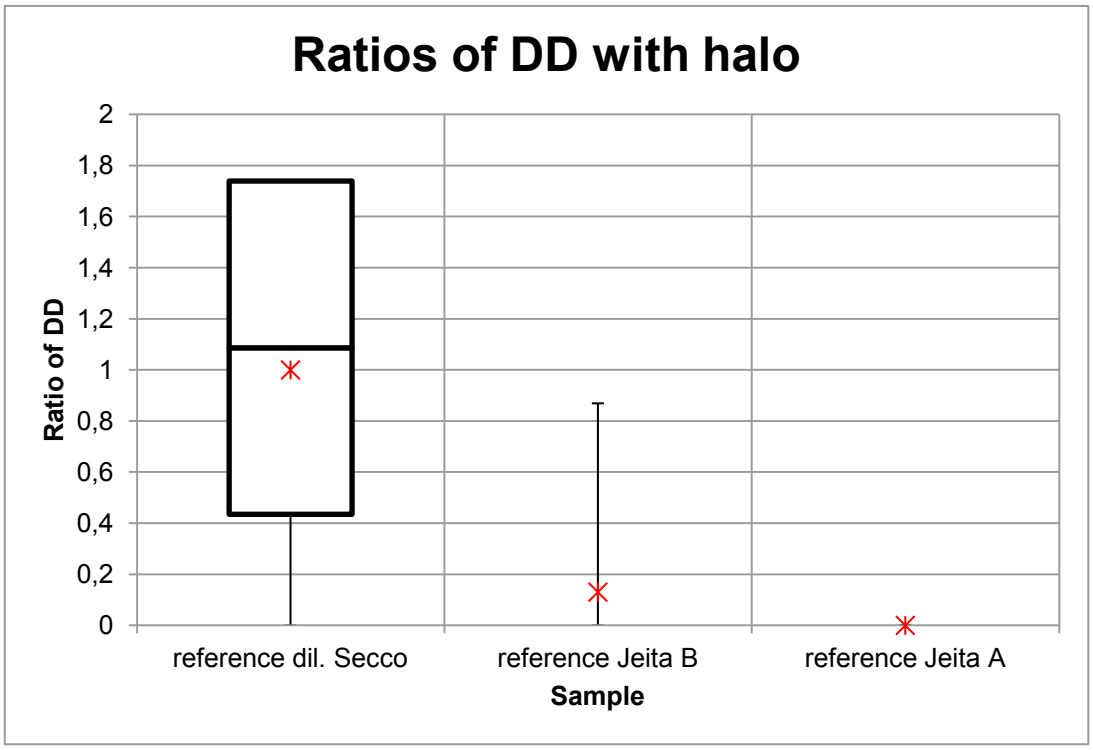


Fig. 3.78 Ratios of densities of defects a) with a halo and b) without a halo on thick SOI fragments etched with Jeita A, decorated with 0.0001–10 ppm Cu, annealed at 950°C. The DD are normalized to the value of Jeita A Ref 1 without halo because no defects with halos could be found in the reference sample.
1 ppm Cu in b): Sharp distribution close to detection limit.

Comparison of the ratios of reference DD using the preferential etching solutions dil. Secco (0.04 M Cr (VI)), Jeita A (without KI) and Jeita B (with KI)

Fig. 3.79 shows a comparison of the ratios of DD of the Ref 1 samples separated into defects with a halo (Fig. 3.79a) and defects without a halo (Fig. 3.79b). For the defects with a halo the DD determined with the dil. Secco (0.04 M Cr (VI)) is the highest. This means that the dilute Secco etch produced more pits with halos than Jeita A and B. An opposite trend was found for the defects without a halo: The DD after etching with Jeita A or B exceed those determined by dil. Secco etch. This indicates that both the higher oxidizing potential and the higher selectivity of the dilute Secco (0.04 M Cr (VI)) result in a better delineation of defects with a halo while Jeita A and B produce a higher DD of pits albeit small and shallow.

a)



b)

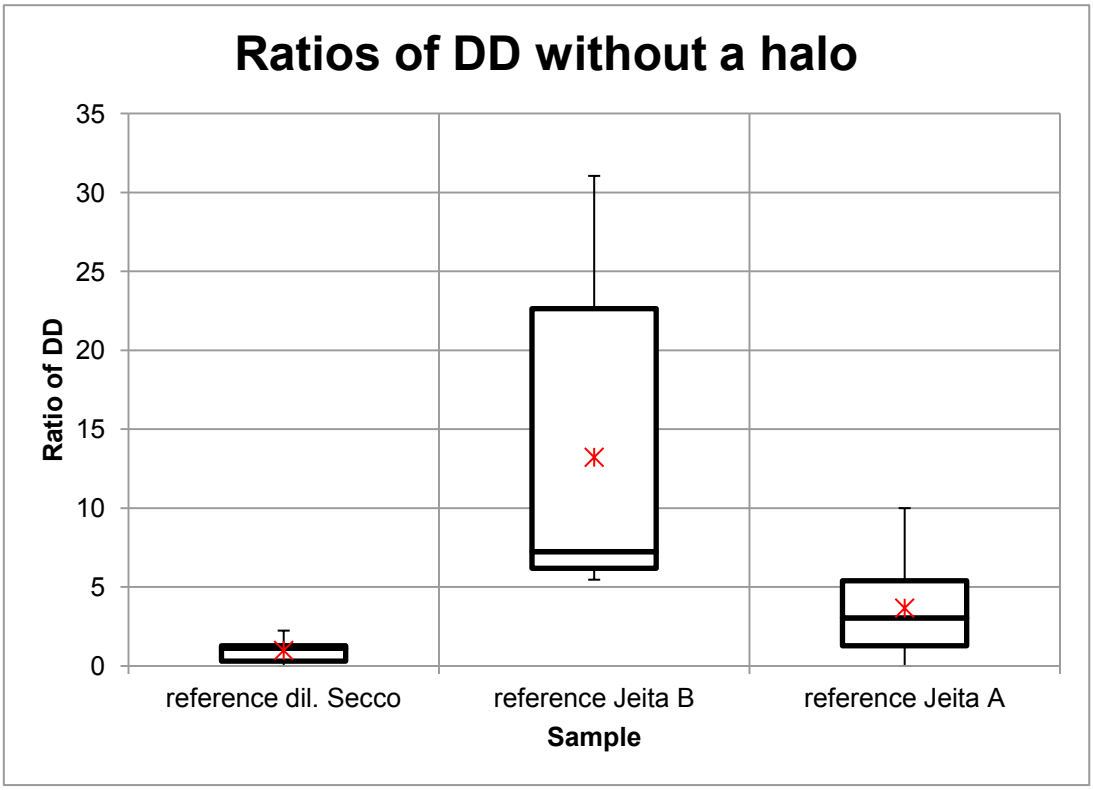


Fig. 3.79 Comparison of the DD ratios of non-decorated thick SOI reference samples: a) with a halo and b) without a halo, etched with dil. Secco (0.04 M Cr (VI)), Jeita A and Jeita B. The DD are normalized to the value of the dil. Secco reference with halo.
Ref (Jeita A) in a): Below detection limit. Ref (Jeita B) in a): Majority of the samples below detection limit with few outliers.

Conclusion for the copper decorated samples:

These results obtained after copper decoration and etching with a dilute Secco (0.04 M Cr(VI)) indicate that copper concentrations around 0.01 to 0.1 ppm provide suitable decoration conditions for defects with and without a halo in 1 400 nm thick SOI.

No clear relationship can be seen between copper concentration and the ratios of defect densities for defects with and without a halo after etching with Jeita A or B. The reason could be both the considerably lower oxidizing potential and the much lower selectivity S of the Jeita etchant compared to that of the dil. Secco (0.04 M Cr (VI)).

3.8.2 610 nm thick SOI

SOI wafers with a silicon film thickness of approx. 610 nm and a BOX thickness of 300 nm were used for these studies. Three different preferential etching solutions were used for the delineation of crystal defects with and without copper decoration (see Tab. 3.10):

- Dil. Secco (0.04 M Cr (VI))
- CP4 + KIO_3 (CP4 A)
- CP4 + KIO_3 + KI (CP4 B)

Detailed information about the recipes of the etchants are given in the appendix.

In addition to dilute Secco etch, two alternative Cr-less solutions were also tested with the 610 nm thick SOI because of their higher etch rates (CP4 A: 1.7 nm/s and CP4 B: 1.9 nm/s) compared to dilute Secco (0.04 M Cr (VI)) (0.6-0.7 nm/s). The uniformity of the sample surfaces was not as smooth as the 90 nm SOI sample surfaces after the etching step. These two newly developed versions of the CP4 (Chemical Polishing Etchant 4) containing KIO_3 or KIO_3 + KI instead of Br_2 as a component were preferred over the Jeita (Jeita A: 4.5 nm/s and Jeita B: 4.7 nm/s) solutions due to their lower etch rate being more suited to the SOI layer thickness of 610 nm.

The etch rate of the original CP4 is 7.5 nm/s at room temperature which is quite high and therefore not applicable for most SOI films. For this reason further additions such as KIO_3 or KIO_3 + KI were tested to replace just bromine as component and therefore keep the main preferential etching characteristics of the etchant [117].

Tab. 3.10 Composition and properties of etching solutions used.

Etching solution	Composition	Etch rate [nm/s]	Oxidizing potential E_0 [mV]
Dil. Secco (0.04 M Cr (VI))	$K_2Cr_2O_7$ H_2O (50%) HF	0.6-0.7	1 330
CP4 + KIO_3	HAc HNO_3 (50%) HF KIO_3	1.7	960 540
CP4 + KIO_3 + KI	HAc HNO_3 (50%) HF KI, KIO_3	1.9	960 540

First the etch rate and the etching temperature were determined at Ref 1 samples to obtain the optimized etching conditions for defect delineation. Experimental conditions such as Cu concentration and annealing temperature in the furnace used for copper decoration were developed and optimized regarding to the 300 nm BOX layer.

However, the 300 nm thick BOX layer in this SOI wafer acts as a strong diffusion barrier for copper. Yet at 900 °C sufficient copper diffuses through the BOX into the SOI layer to decorate the defects.

Copper decoration was accomplished as described in the foregoing experiments but with the fragments annealed at 900 °C for 1 min (No Ref 2 samples were prepared for these experiments). This was followed by etching the SOI layer down to a thickness of 78-185 nm with the preferential etchants used. The etch rates and the oxidizing potentials of the etching solutions used are illustrated in Tab. 3.10, both etching duration and the duration of the dip in HF are shown in Tab. 3.11.

A dip in HF for 90 s for the dilute Secco and for 5 min for both CP4 solutions served to etch the buried oxide below the pits thus producing a halo under an optical light microscope. The dip in HF was needed to be much longer for the CP4 A and CP4 B to produce a halo of sufficient size at the pits to obtain good results for their delineation. Further characterisation of selected defects was performed via SEM.

Based on the defect delineation procedures using these etching solutions the DD were determined for etch pits with a halo.

Tab. 3.11 Etching conditions of the etching solutions used.

Etching solution	Etching duration	HF dip
Dil. Secco (0.04 M Cr (VI))	**13 min**	**90 s**
CP4 + KIO_3	**5 min 10 s**	**5 min**
CP4 + KIO_3 + KI	**4 min 30 s**	**5 min**

Copper decoration with preferential etching using dil. Secco 0.04 M Cr (VI)

Fig. 3.80 shows a light optical micrograph of a non-decorated Ref 1 sample. Defects with a halo ("1") and few without a halo ("2") are visible. Etch pits with a halo offer bright rings around the pits which indicate their extension. The interference colours are caused by the light optical microscope due to the contrasts arising from the thick SOI film which is still intact and collapsed in a stepped way. Just few pits without a halo as dark contrasts were found. At some magnified defects a circle was drawn for the determination of the pits radius.

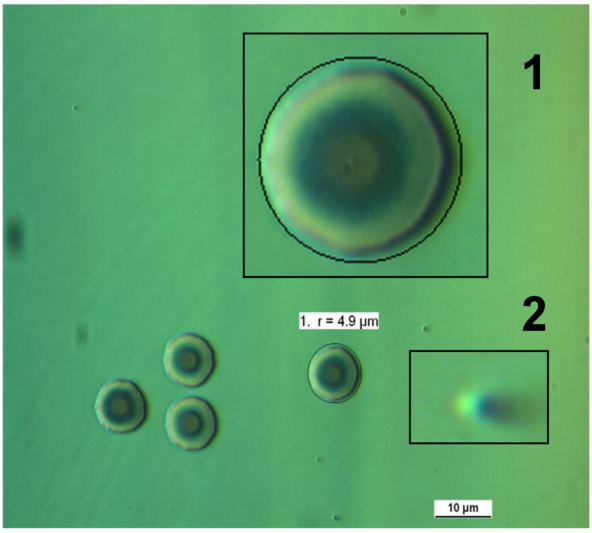


Fig. 3.80 Light optical micrograph of a 610 nm thick SOI Ref 1 sample, etched with dil. Secco (0.04 M Cr (VI)) and dipped in HF for 90 s; residual layer thickness: approx. 119 nm. Magnified view in inserts. Pits with halo ("1") and pits without halo ("2") are displayed.

Fig. 3.81 presents a copper decorated and etched sample. The sample was decorated with [Cu] = 0.1 ppm and annealed at 900 °C. Defects with a bright halo are visible. Again the SOI film at the etch pits is still intact. Mentionable is the different size of the decorated etch pits. These could be copper decorated oxygen precipitates which look like COPs and lie in deeper parts of the SOI film. Few defects without a halo could be detected.

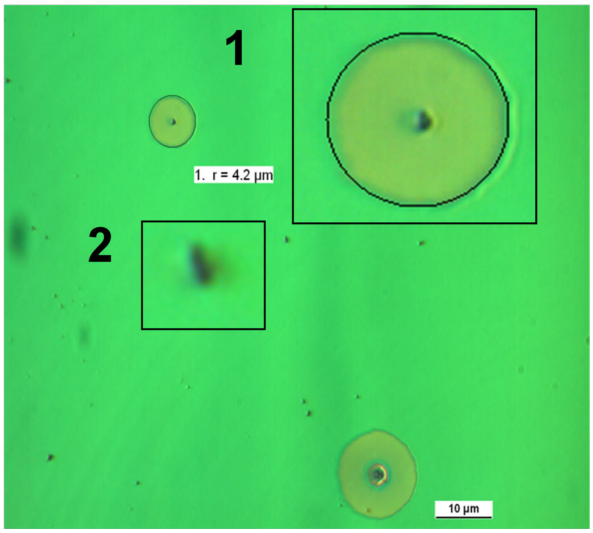


Fig. 3.81 Light optical micrograph of a 610 nm thick SOI sample decorated with 0.1 ppm copper, annealed at 900 °C, etched with dil. Secco (0.04 M Cr (VI)) and dipped in HF for 90 s; residual layer thickness: approx. 117 nm. Magnified view in inserts. Pits with halo ("1") and pits without halo ("2") are displayed.

Fig. 3.82 displays a light optical micrograph of a SOI sample decorated with 10 ppm copper. A high density of etch pits with a halo is visible. Some of the defects exhibit a ring-like colored image due to the interference contrast produced in the light optical microscope. This underlines the step-like collapse of the SOI film down to the substrate at some etch pits. At the rather single-coloured etch pits the SOI film collapsed more uniformly. Some additional details of the etch features at the defects can be taken from the SEM image (Fig. 3.83).

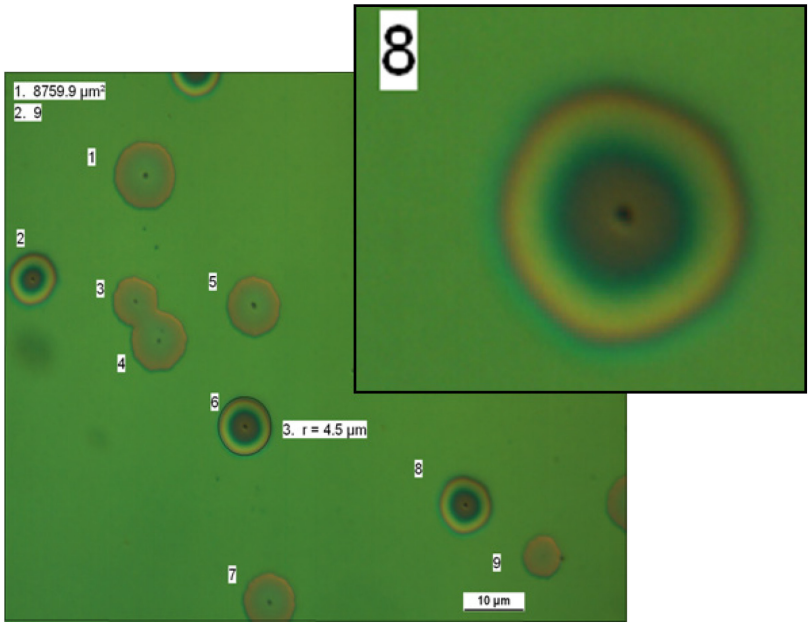


Fig. 3.82 Light optical micrograph of a 610 nm thick SOI sample decorated with 10 ppm copper, annealed at 900 °C, etched with dil. Secco (0.04 M Cr (VI)) and dipped in HF for 90 s; residual layer thickness: approx. 120 nm. Magnified view in insert. Pits with halo and a few pits without halo are displayed.

Fig. 3.83 shows a SEM image of a SOI sample (decorated with 10 ppm copper) and delivers insight into the etch features of a defect with a halo. In the center the location of the original defect is revealed. The undercut BOX and the collapsed SOI film (areas with dark gray contrast) are clearly visible. A part of the SOI film was split and broke off, very likely due to the vacuum in the SEM during the SEM investigation. The origin of the white double-ring in the area without SOI film is not clear. It could have been produced by etching off a thin silicon layer of the SOI carrier wafer by an electrochemical etching process in which copper and HF interact with the silicon.

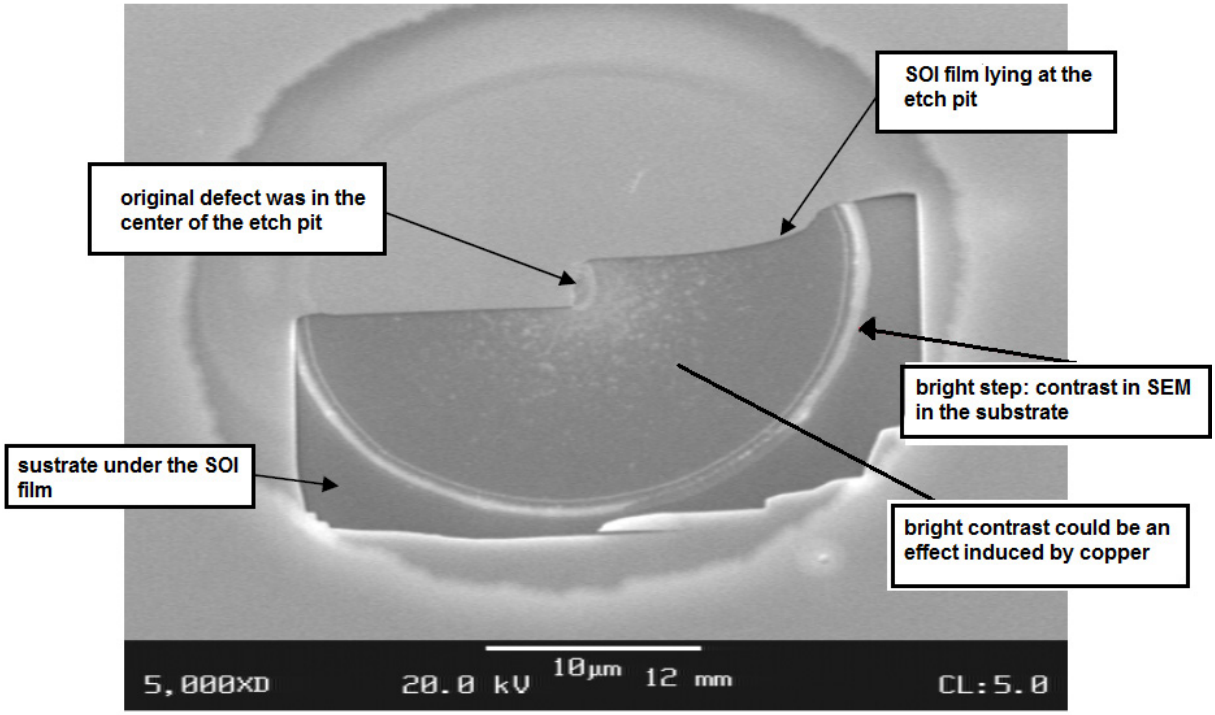


Fig. 3.83 SEM of a 610 nm thick SOI sample decorated with 10 ppm copper, annealed at 900 °C, etched with dil. Secco (0.04 M Cr (VI)) and dipped in HF for 90 s; residual layer thickness: approx. 120 nm. Additional details of the etch feature in inserts.

The diagrams in Fig. 3.84 illustrate the measured radii for non-decorated and copper decorated defects with a halo after annealing at 900 °C. The average radius obtained for the Ref 1 samples was 4.9 µm. The copper decoration step causes an enhancement of the defects. Therefore, the average values for the radii determined after copper decoration were slightly higher (4.2–6.6 µm).

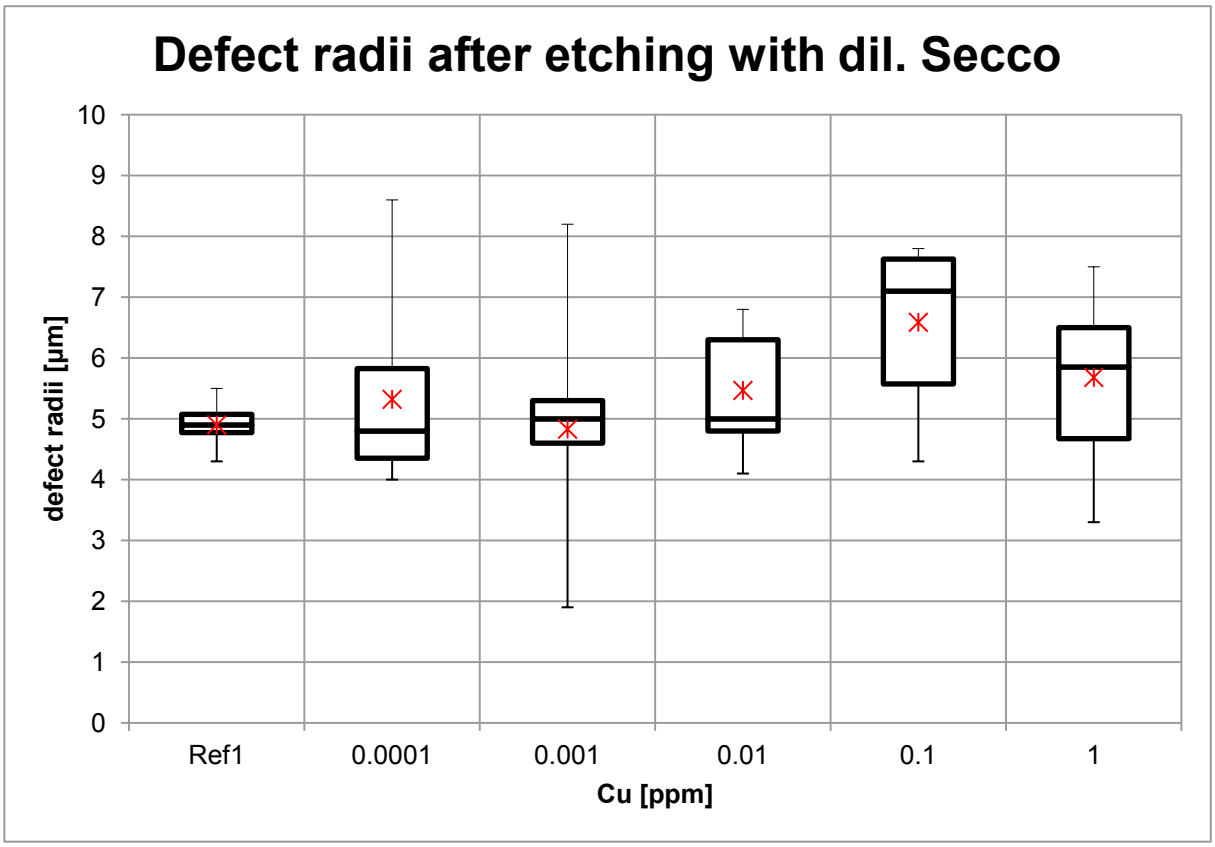


Fig. 3.84 Comparison of the average radii of the etch pits with a halo after etching with dil. Secco 0.04 M Cr (VI). Error bars show the standard deviation.

The diagrams in Fig. 3.85 show the densities of etch pits with a halo of Ref 1 and copper decorated samples etched with a dilute Secco (0.04 M Cr (VI)). A slight increase in DD is indicated although not significant according to the error bars after using a copper concentration of [Cu] ≥ 0.1 ppm. It may thus be concluded that the required [Cu] is ≥ 0.1 ppm to decorate the defects in 610 nm SOI.

Defects without a halo could scarcely be observed and there was no increase in DD after copper decoration, hence, no diagram was created for their density.

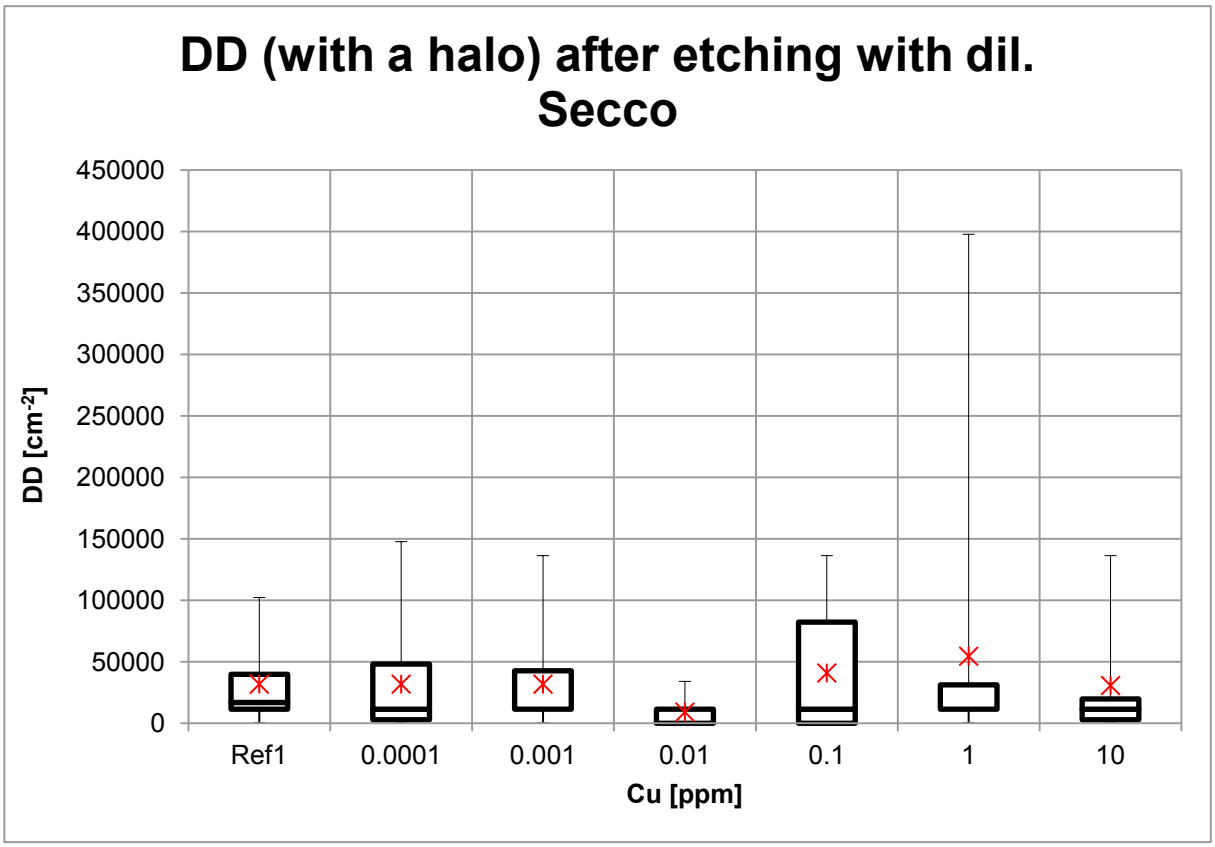


Fig. 3.85 Ratios of DD of etch pits with halos on 610 nm thick SOI decorated with copper, annealed at 900°C, etched with dil. Secco (0.04 M (Cr (VI)) and dipped in HF for 90 s.
0.001 and 1 ppm Cu: Second quantel coincides with median. 0.01 ppm Cu: Majority of the samples below detection limit with few outliers.

Copper decoration with preferential etching using CP4 A and B

A much higher DD was determined after etching with a dil. Secco compared to the CP4 A and B etching solutions. The DD after using a CP4 A were twice as high as after etching with CP4 B. It can be concluded that both CP4 etching solutions are not suitable to detect all defects in these thick SOI fragments. A reason could be the lower selectivity of the CP4 A and CP4 B etching solutions compared to diluted Secco etch and/or the lower oxidizing potential of the CP4 etching solutions. Therefore the erratic results of both etching solutions CP4 A and B are not covered in detail here.

Conclusion

A slight increase in DD was observed using a copper concentration of [Cu] ≥ 0.1 ppm after etching with a dil. Secco (0.04 M Cr (VI)). Hence, it can be concluded that the required [Cu] is ≥ 0.1 ppm to decorate the defects in 610 nm SOI.

3.9 Delineation of crystal defects in SIMOX wafers

Copper decoration and preferential etching studies were also performed on SIMOX wafers [118] for the delineation and characterisation of crystal defects such as COPs (Crystal Originated Particles) and oxygen precipitates [119]. The material used was from a relatively old batch of heavily scratched SIMOX wafers.

The SOI-films used had a layer thickness of 200 nm, the thickness of the buried oxide (BOX) was 95 nm. Copper decoration was accomplished by furnace annealing at 800 °C (see section 3.1). The Ref 1 a–c and copper decorated samples were etched with a dilute Secco 0.04 M Cr (VI) using different etching times resulting in different residual layer thicknesses (LT_{res}) to analyse the density of etch pits in the whole SIMOX film (see Tab. 3.12). Ref 1 (d) samples were etched with an OPE B as a chromium–free alternative etching solution. OPE B was selected because its etch rate on SIMOX wafers (0.29 nm/s) was close to that of dil. Secco (0.04 M Cr (VI)) (0.65 nm/s). This was followed by a dip in HF for 90 s to etch the buried oxide below the pits and produce a halo under an optical light microscope. Detailed information on the etchants are given in the appendix.

Tab. 3.12 Comparison of average DD of Ref 1 (a – c) and copper decorated 200 nm SIMOX samples, etched with dil. Secco 0.04 M Cr (VI). Ref 1(d) samples were etched with OPE B. All sampled were dipped in HF for 90 s. t: etching duration; LT_{res}: average residual layer thickness.

Cu-conc. [ppm]	t [s]	LT_{res} [nm]	DD [cm^{-2}]
0 (Ref 1, d)	312	109.8	DD_{mean} 9 400 DD_{max} 25 500 DD_{min} 0
0 (Ref 1, c)	295	18.9	DD_{mean} 117 000 DD_{max} 520 800 DD_{min} 16 900
0 (Ref 1, b)	252	37.1	DD_{mean} 6 200 DD_{max} 8 500 DD_{min} 2 800
0 (Ref 1, a)	220	55.5	DD_{mean} 7 800 DD_{max} 27 900 DD_{min} 0
0.1	220	72.8	DD_{mean} 19 000 DD_{max} 82 100 DD_{min} 0
1	220	66.1	DD_{mean} 47 900 DD_{max} 138 800 DD_{min} 8 500
10	220	69.5	DD_{mean} 17 400 DD_{max} 50 900 DD_{min} 0

Tab. 3.12 and the diagram in Fig. 3.86 show the comparison of the average DD of the etch pits determined for Ref 1 and copper decorated SIMOX samples. For the Secco etched Ref 1 a-c a distinct increase of DD with decreasing LT_{res} is obvious. Most of the defects seem to be located in the zone close to the BOX. However, the explanation is as follows: The lower LT_{res} the more etch pits due to defects of a certain size reach down to the BOX giving rise to a halo in the subsequent HF treatment. One may conclude that the initial layer thickness should be etched down to values lower than 20 nm for the LT_{res} to reveal all defects in SIMOX. Very likely the majority of the defects are process-induced oxygen precipitates. They have been generated during the annealing step following the oxygen implantation in which the BOX is formed and the implantation-induced damage is removed.

The DD (DD_{mean} = 9 400 cm^2) determined after etching with OPE B (LT_{res}: 109.8 nm) was comparable to the DD (DD_{mean} = 7 800 cm^2) obtained for the samples etched with dilute Secco (Ref 1, a; LT_{res}: 55.5 nm). OPE B appears to be a good chromium-free alternative for defect delineation in SIMOX. The DD increases after Cu decoration for samples with a LT_{res} of 66-73 nm compared to the DD obtained for the references with a similar LT_{res} (Ref 1, a).

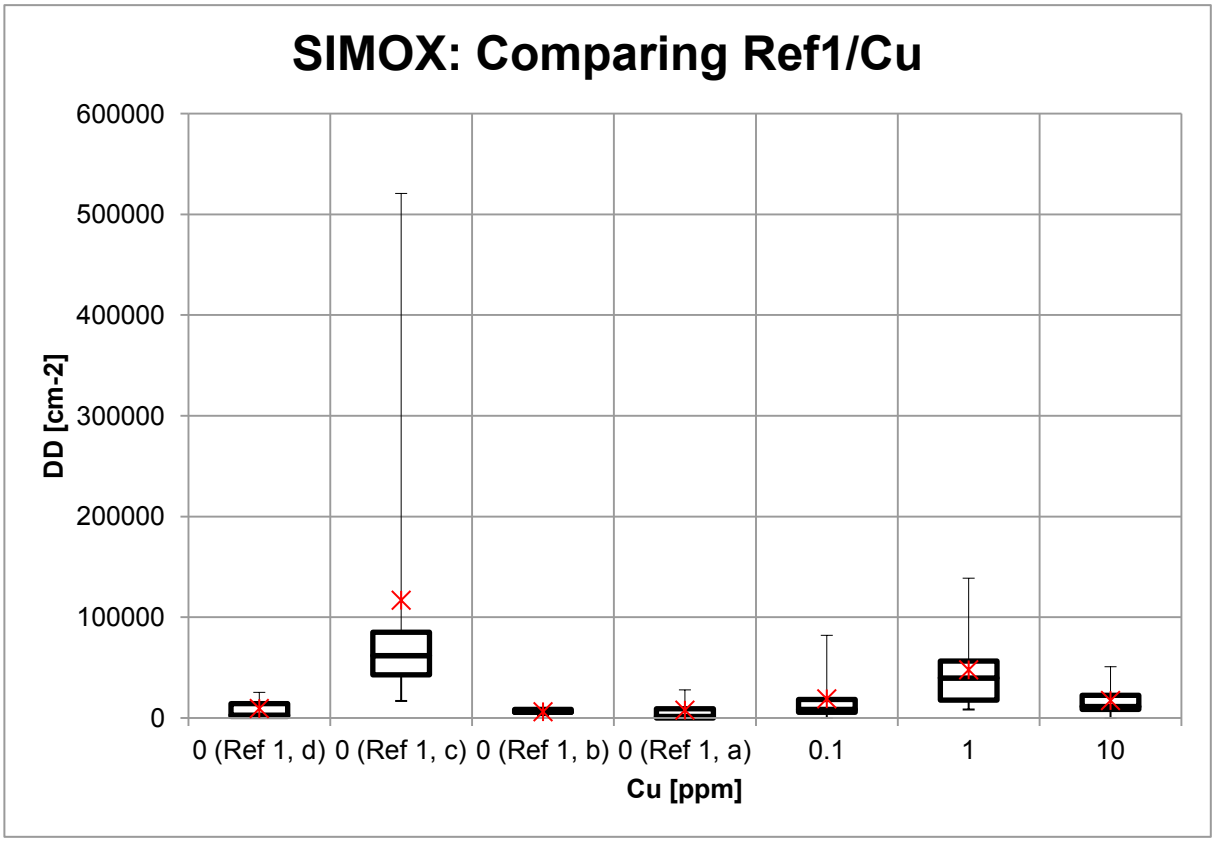


Fig. 3.86 DD of etch pits on 200 nm SIMOX of Ref 1(a – d) and copper decorated samples, annealed at 800 °C, etched with dil. Secco 0.04 M Cr (VI) and dipped in HF for 90 s. Ref 1 (d) was etched with an OPE B. For LTres values see Tab. 3.12.

The light optical micrographs in Fig. 3.87 (Ref 1, a) and Fig. 3.88 (Ref 1, c) show Ref 1 samples with different residual layer thicknesses etched with a dilute Secco. Only dark defect etch features (halos) with a faint dot in the center were detected. In the case of defects with such completely dark features on the surface the residual SOI film had collapsed down to the substrate. The DD is significantly higher for SIMOX layers with a lower LT_{res} (Fig. 3.88). Only one dark defect could be determined in Fig. 3.87.

The etched SIMOX surface was inhomogeneous in all characterised samples due to the damage caused by the oxygen implantation procedure. This leads to difficulties in the examination and counting of defects in some light optical micrographs.

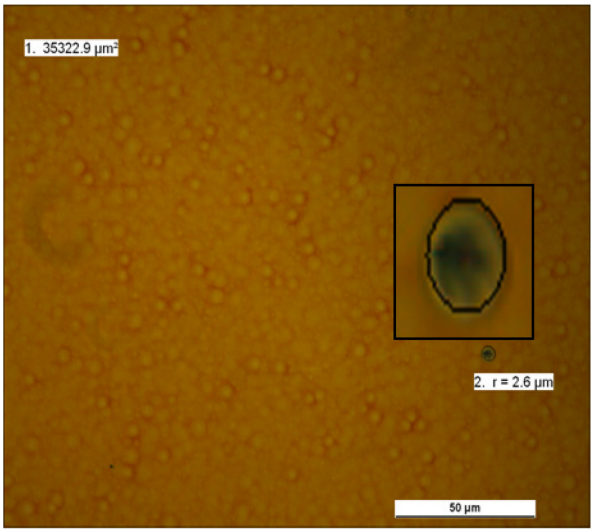


Fig. 3.87 Light optical micrograph of a 200 nm SIMOX Ref 1 (a) sample, etched with dil. Secco (0.04 M Cr (VI)) and dipped in HF for 90 s, residual layer thickness: 55.5 nm. One defect visible.

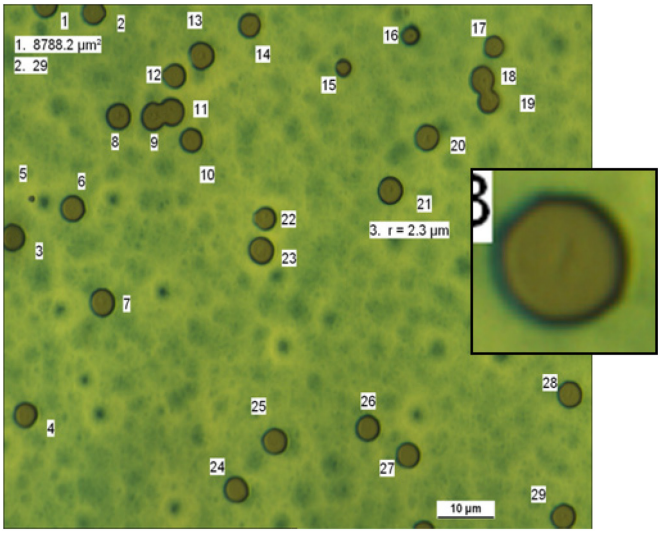


Fig. 3.88 Light optical micrograph of a 200 nm SIMOX Ref 1(c) sample, etched with dil. Secco (0.04 M Cr (VI)) and dipped in HF for 90 s, residual layer thickness: 18.9 nm. High DD. Magnified view in insert.

SEM images of a Ref 1 sample with LT_{res} of 18.9 nm were taken for a detailed investigation of the defects (Fig. 3.89). The right image presents a magnified view of a defect exhibiting a halo and an etch pit in the centre. The low LT_{res} of the sample resulted in a shallow etch feature at the defect and in the collapse of the residual SOI film. The shallow etch feature may be ascribed to the low LT_{res} of the sample.

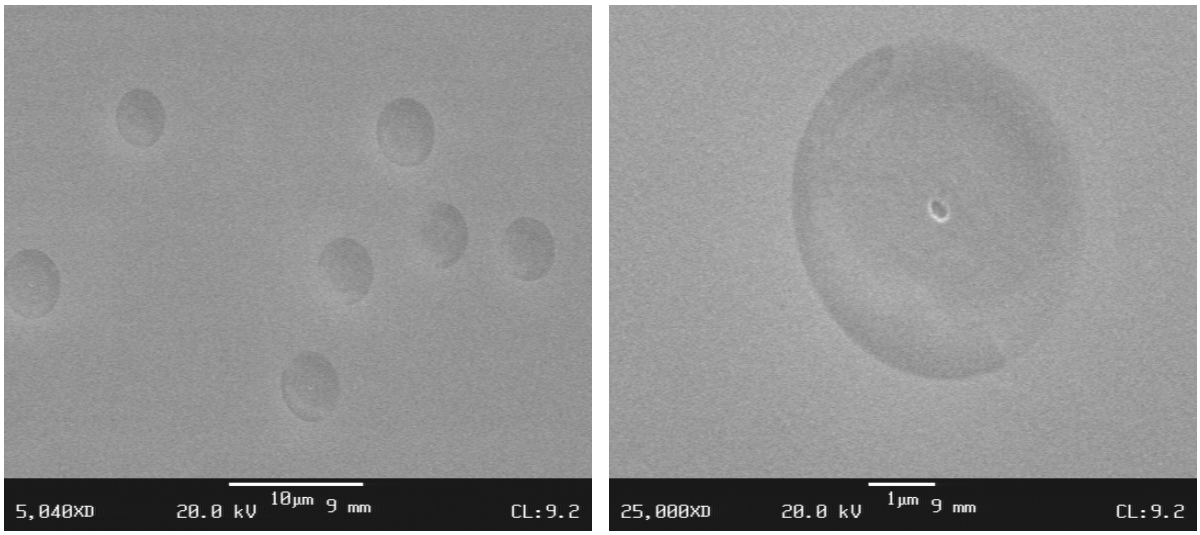


Fig. 3.89 SEM images of a 200 nm SIMOX Ref 1(c) sample etched with dil. Secco (0.04 M Cr (VI)) and dipped in HF for 90 s, residual layer thickness: 18.9 nm. Same sample as in Fig. 3.88.

The light optical micrographs in Fig. 3.90 (0.1 ppm Cu) and 3.91 (10 ppm Cu) show copper decorated samples which were etched with a dilute Secco. The defects in Fig. 3.90 exhibit a dark area in the centre surrounded by a bright halo. The dark area of the defect is the

residual silicon layer which collapsed down to the substrate. Fig. 3.91 shows a sample decorated with a high copper concentration. The ion implantation step in the SIMOX process leads to a highly damaged silicon crystal lattice. Process-induced damages could be detected in the deeper parts and not at the SIMOX sample surface. Precipitation of copper could have occurred at ion implantation damages producing the reddish brown dots in this light optical micrograph. The even distribution of the reddish brown dots may be attributed to copper decorated damages instead of artefacts which would appear in an insular distribution in random isolated groups. The defects appear brighter. However, the SIMOX silicon layer at the etch pits did not collapse down to the substrate.

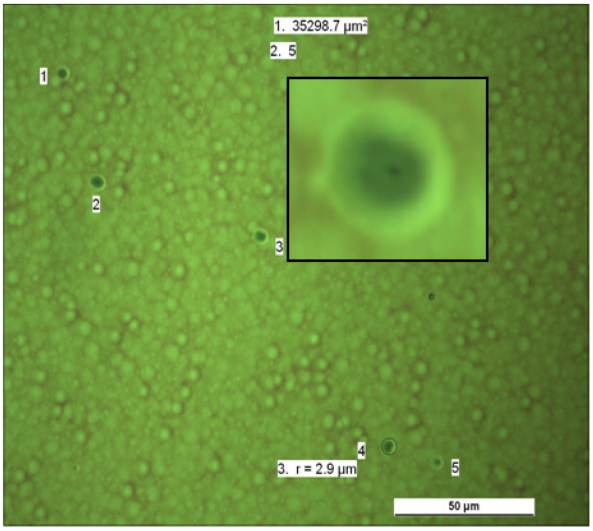


Fig. 3.90 Light optical micrograph of a 200 nm SIMOX sample decorated with 0.1 ppm copper, annealed at 800 °C, etched with dil. Secco (0.04 M Cr (VI)) and dipped in HF for 90 s; residual layer thickness: 64.7 nm. Several defects visible; magnified view of one defect in insert.

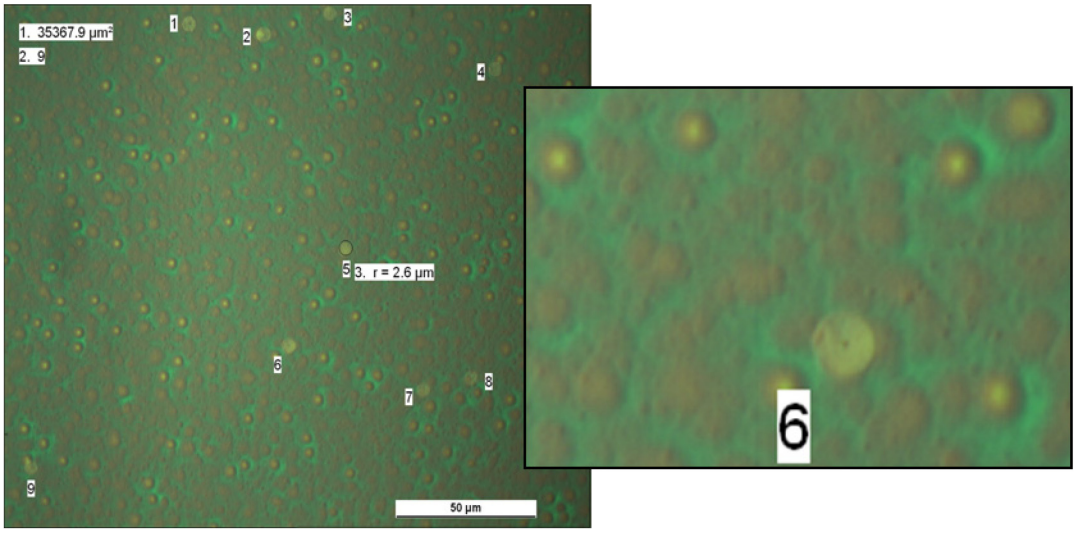


Fig. 3.91 Light optical micrograph of a 200 nm SIMOX sample decorated with 10 ppm copper, annealed at 800 °C, etched with dil. Secco (0.04 M Cr (VI)) and dipped in HF for 90 s, residual layer thickness: 74.1 nm. Magnified view in insert. High DD and a high density of reddish brown dots.

Conclusion

In SIMOX most of the defects seem to be located in the zone close to the BOX. Therefore, the silicon film should be etched down to values lower than 20 nm to delineate all defects. Very likely the majority of the defects are process-induced oxygen precipitates which may be formed during the high temperature annealing step after the oxygen implantation for the BOX formation and removal of the lattice damage. After decoration of these defects with copper their density detected by preferential etching increased. With [Cu] = 10 ppm a high density of evenly distributed reddish brown dots was observed. This effect is caused by the decoration of the highly damaged silicon crystal lattice with copper.

OPE B was tested as a chromium-free alternative etching solution on the basis of it's etch rate. This solution seems to be a good alternative for defect delineation in SIMOX. The DD obtained were in the same range as the DD obtained after etching with a dilute Secco etch. However, the material used was from a relatively old batch of heavily scratched SIMOX wafers. Therefore no further copper decoration experiments using OPE B for defect etching were performed.

3.10 Copper decoration and preferential etching of crystal defects in sSOI materials

3.10.1 OPE etching solutions used

The chromium-free OPE solutions [112, 120] delineate threading dislocations (TD) but not stacking faults (SF). An attempt was therefore made to combine copper decoration with preferential etching using different OPE solutions to reveal both stacking faults and threading dislocations in sSOI materials [121].

Various OPE solutions were tested to achieve the best defect delineation (Tab. 3.13):

Tab. 3.13 Etch rates of OPE solutions used.

Etching solution	Etch rate [nm/min]
OPE A	0.60
OPE B	0.54
OPE D	1.29
OPE F	1.74

The influence of copper decoration on the etch rate was determined first, using the OPE D solution to etch 65 nm sSOI samples down to the BOX at room temperature (23 °C). Non-decorated reference samples (Ref 1) were etched with OPE D and the etch rates were determined and compared to the etch rates of samples decorated with 0.1 and 10 ppm Cu and etched with OPE D. Tab. 3.14 shows the etch rates obtained.

Tab. 3.14 Etch rates measured for Ref 1 and Cu-decorated samples etched with OPE D.

Cu [ppm]	Etch rate [nm/min]
Ref 1	1.29
0.1	1.54
10	1.53

These experiments show that copper decoration leads to an increase of the etch rate of OPE D of about 19% in sSOI samples. Interestingly, there is practically no difference in the etch rates obtained after copper decoration with 0.1 ppm Cu and 10 ppm Cu. Hence, it can be assumed that the copper decoration itself causes an increased etch rate independent of the metal concentration used within these limits.

3.10.2 OPE D

A combination of copper decoration and OPE D etching was tested for the delineation of both types of crystal defects (TDs and SFs) in sSOI.

The sSOI wafer had an initial layer thickness of 65 nm (sSOI) and a BOX layer thickness of 145 nm. Some of the sSOI fragments were only etched with OPE D for 18 min at room temperature (23 °C). A HF dip was not necessary to etch the BOX below the pits. A second batch of the sSOI fragments was decorated only with copper concentrations of 0.1, 1.0 and 10 ppm, owing to the limited number of 65 nm sSOI wafers at our disposal. This was followed by preferential etching with OPE D for 18 min at room temperature as with the Ref 1 samples. A residual layer thickness of about 35-40 nm was measured for all fragments. Copper decorated and Ref 1 fragments were compared.

Fig. 3.92 shows a light optical micrograph of a Ref 1 sample. Only threading dislocations are visible. A few bright etched TD show an intact sSOI film. The dark pits are those in which the sSOI film has sunk to the substrate. Stacking faults could not be detected in the reference samples.

A circle was drawn around some pits of selected samples for the determination of their radii. The delineated crystal defects differ in their radii, which were measured to get an idea of the distribution of the defects in the film. Defects which occur at the upper part of the film form pits with larger radii, as they are etched longer than those deeper in the film.

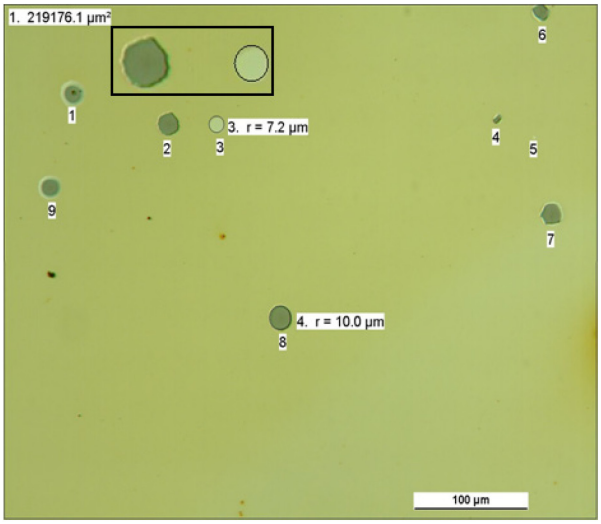


Fig. 3.92 A light optical micrograph of a 65 nm Ref 1 sSOI sample etched with OPE D; residual layer thickness: 39 nm. TD with different radii are visible. Magnified view in insert. At some magnified defects a circle was drawn for the determination of the pit radius.

Fig. 3.93 shows a sSOI fragment decorated with 0.1 ppm Cu and having a very high defect density of threading dislocations. A copper concentration of 0.1 ppm leads to a significant increase of the TD defect density. Several threading dislocations appear to possess screw components in varying degrees. This is due to the fact that sSOI is a lattice mismatched film and as such contains crystal defects like misfit and threading dislocations, stacking faults and screw dislocations. There were no stacking faults to be seen.

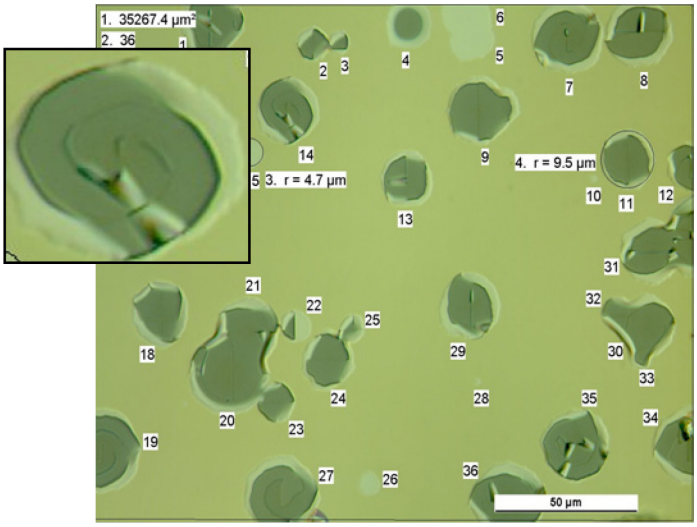


Fig. 3.93 Light optical micrograph of a 65 nm sSOI sample, decorated with 0.1 ppm Cu, etched with OPE D; residual layer thickness: 37 nm. High DD of TD. Some spiral features are visible which are interpreted as TD with screw components. Magnified view in insert. At some magnified defects a circle was drawn to determine the pit radius.

A copper concentration of 10 ppm did not result in a much higher defect density or in the delineation of stacking faults compared to the lower copper concentrations used (Fig. 3.94).

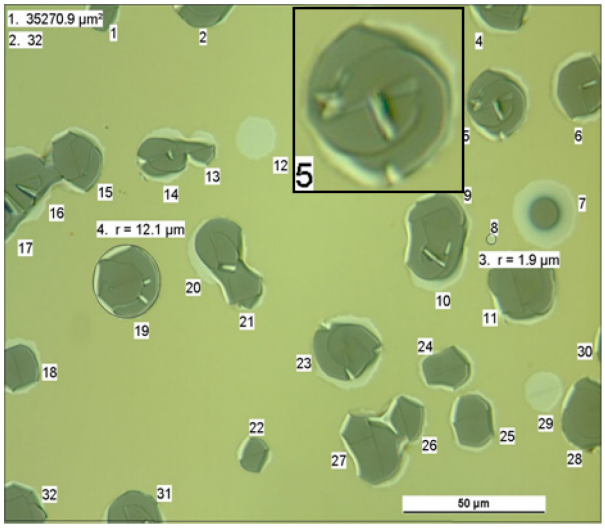


Fig. 3.94 Light optical micrograph of a 65 nm sSOI sample, decorated with 10 ppm Cu, etched with OPE D; residual layer thickness: 38 nm. High DD of TD. Some spiral features attributed to screw dislocations are also visible. Magnified view in insert. At some magnified defects a circle was drawn for the determination of the pit radius.

Conclusion

Even in combination with copper decoration, OPE D etching did not delineate stacking faults in sSOI layers, only threading dislocations were delineated

3.10.3 OPE A

A combination of copper decoration and OPE A etching was tested for its ability to reveal both threading dislocations and stacking faults in sSOI.

The sSOI wafer had an initial layer thickness of 65 nm (sSOI) and a BOX layer thickness of 145 nm. Some of the sSOI fragments were just etched with OPE A for 30 min at room temperature (23 °C). A dip in HF for 1 min served to etch the BOX below the pits. Thus the defects were easily detected under an optical light microscope.

A second batch of the sSOI fragments were first copper decorated with 0.5 µL of a $Cu(NO_2)_3$ solution containing the selected copper concentrations 0.1, 1.0 and 10 ppm followed by annealing at 800 °C for 1 min in the furnace. Copper decoration was followed by preferential etching with OPE A for 30 min and a dip in HF for 1 min at room temperature. A residual layer thickness of about 45-55 nm was measured for all fragments. Copper decorated and

Ref 1 fragments were characterised and compared. The etch rates increased significantly after copper decoration (Tab. 3.15).

Tab. 3.15 Etch rates of Ref 1 and Cu-decorated samples etched with OPE A.

Cu [ppm]	Etch rate [nm/min]
Ref 1	0.33
0.1	0.66
1	0.53
10	0.53

Threading dislocations and a screw dislocation-type feature could be detected in the Ref 1 sample (Fig. 3.95) but not any stacking faults.

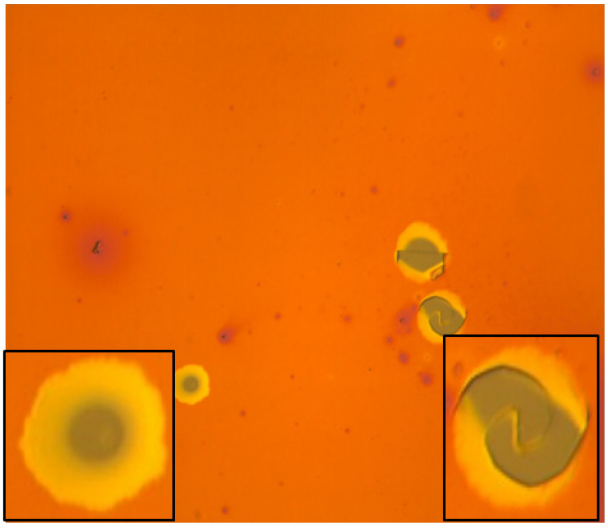


Fig. 3.95 Light optical micrograph of a 65 nm Ref 1 sSOI fragment, etched with OPE A; residual layer thickness: 55 nm. Only TDs and a screw dislocation-type feature are visible. Magnification: 500x.

Fig. 3.96 (0.1 ppm Cu) and Fig. 3.97 (10 ppm Cu) show copper decorated and etched sSOI fragments with very high defect densities of threading dislocations compared to the reference (Fig. 3.95). A copper concentration of 0.1 ppm Cu seems to be enough to cause a significant increase of the TD defect density. Screw dislocation-type features were also detected and are more clearly visible in their structure after decoration with a copper concentration of 0.1 ppm. Such features were not observed at a copper concentration of 10 ppm.

No stacking faults could be observed. A copper concentration of 10 ppm Cu did not lead to a further increase in defect density.

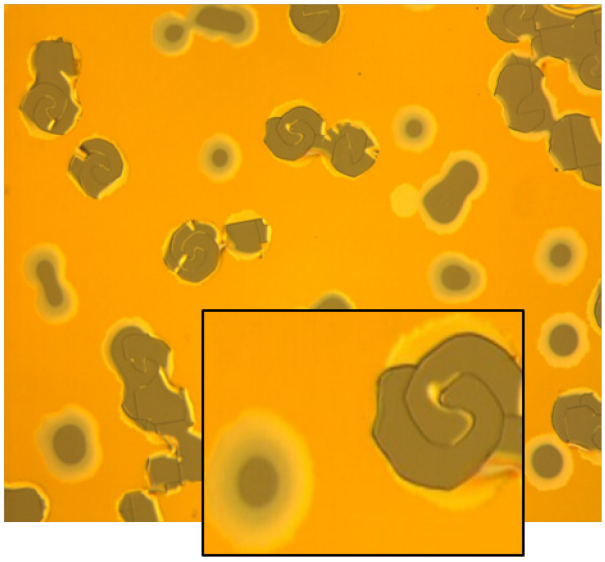


Fig. 3.96 A light optical micrograph of a Cu decorated (0.1 ppm Cu) 65 nm sSOI fragment etched with OPE A is shown. Initial layer thickness: 65 nm, residual layer thickness: 45 nm. Only TDs and screw dislocation-type features are visible. Magnification: 500x.

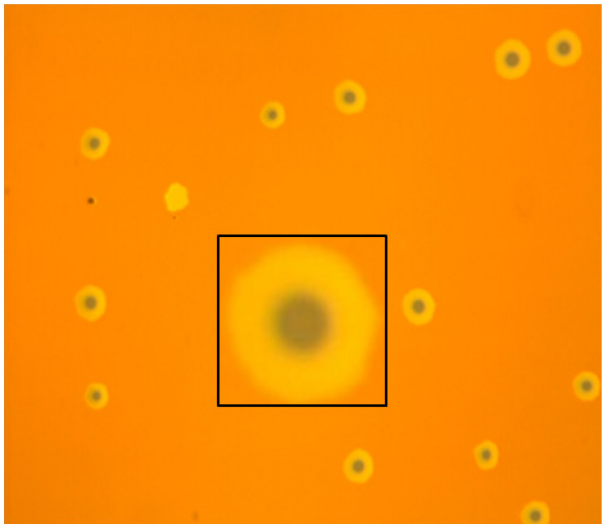


Fig. 3.97 Light optical micrograph of a 65 nm sSOI sample, decorated with 10 ppm Cu, etched with OPE A; residual layer thickness: 49 nm. Only TDs with a higher DD are visible. Magnification: 500x.

Conclusion

The OPE A etching solution in combination with copper decoration is also not able to delineate stacking faults in sSOI layers. Again only threading dislocations were revealed.

3.10.4 OPE F

A combination of copper decoration and OPE F etching was performed to reveal both threading dislocations and stacking faults in sSOI.

As the sSOI wafers with a film thickness of 65 nm had been used up and further samples were not available to us, thin sSOI wafers with a film thickness of 15.6 nm and a box layer of 140 nm were used.

One batch of the sSOI fragments was just etched with OPE F for 10 min at room temperature (24 °C). A dip in HF for 1 min served to etch the BOX below the pits. The defects could easily be characterised using a light optical microscope.

A second batch of sSOI fragments were decorated with copper in concentrations ranging from 0.01–100 ppm as 15.6 nm thick sSOI wafers were readily available. The fragments were then furnace annealed at 800 °C for 1 min in a quartz tube and quenched in air to room temperature. Copper decoration was followed by preferential etching with OPE F for 10 min and a dip in HF at room temperature. A residual layer thickness of about 6-9 nm was measured for all fragments. Copper decorated and Ref 1 fragments were characterised and compared.

Fig. 3.98 shows a Ref 1 sample with a high defect density of dark dots corresponding to threading dislocations. No stacking faults were revealed.

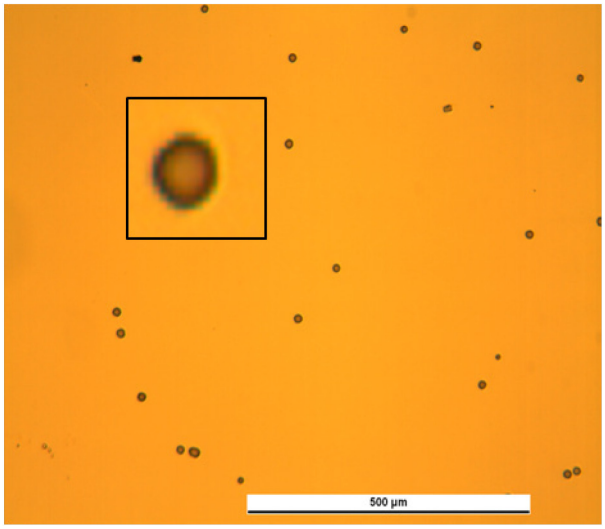


Fig. 3.98 Light optical micrograph of a 15.6 nm Ref 1 sSOI fragment, etched with OPE F; residual layer thickness: 8.9 nm. Only dark dots (TDs) are visible.

The light optical micrograph in Fig. 3.99 shows a copper decorated (0.1 ppm Cu) thin sSOI fragment etched with OPE F. Copper decoration caused a significant increase in the defect

density of dark dots which may correspond to threading dislocations. Etch features attributable to either screw dislocations or stacking faults could not be detected in this sample.

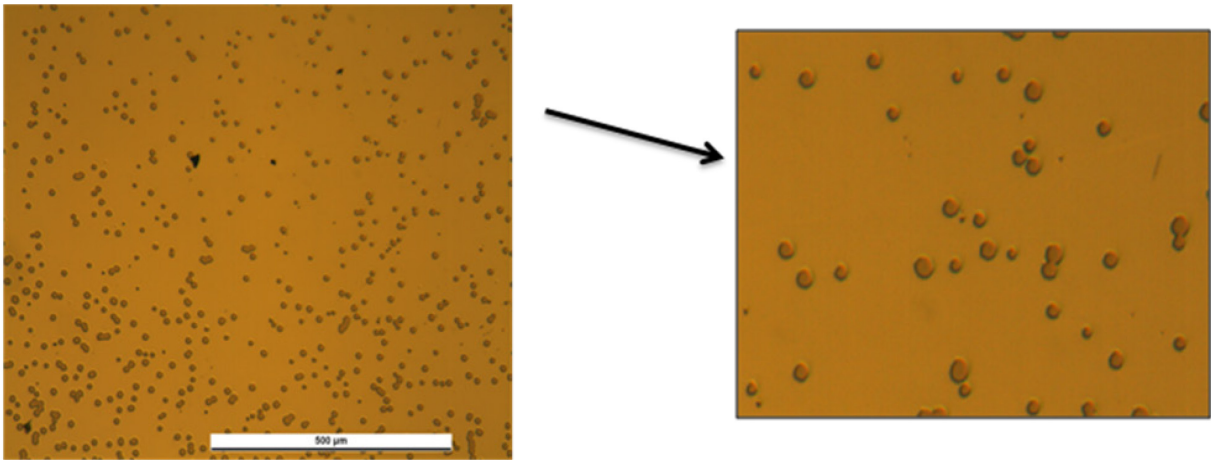


Fig. 3.99 Light optical micrograph of 15.6 nm sSOI fragment, decorated with 0.1 ppm Cu, etched with OPE F; residual layer thickness: 8.4 nm. Only dotlike features which may be attributed to TDs are visible. Magnified view on the right.

A copper concentration of 10 ppm led to a density of dark dots (Fig. 3.100) which is comparable to the DD in samples with lower copper concentrations.

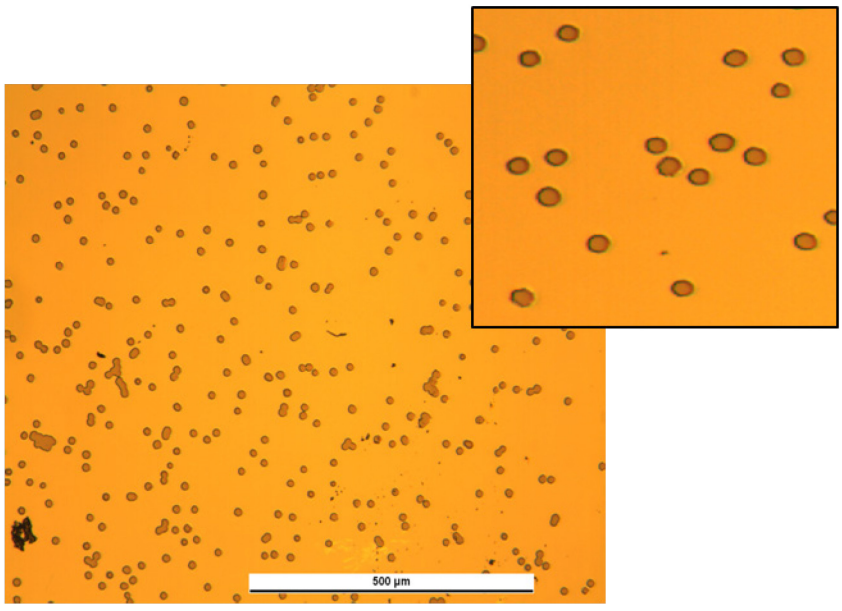


Fig. 3.100 Light optical micrograph of a 15.6 nm sSOI sample, decorated with 10 ppm Cu, etched with OPE F; residual layer thickness: 7.3 nm. Only dotlike features which may be attributed to TDs are visible. Magnified view of the arrays of dots on the right side.

Fig. 3.101 shows a very high density of artefacts in a fragment decorated with 100 ppm Cu and etched with OPE F. Their density is too high to be characterised as stacking faults or

threading dislocations and are more likely an indication of the presence of artefacts induced by copper precipitation.

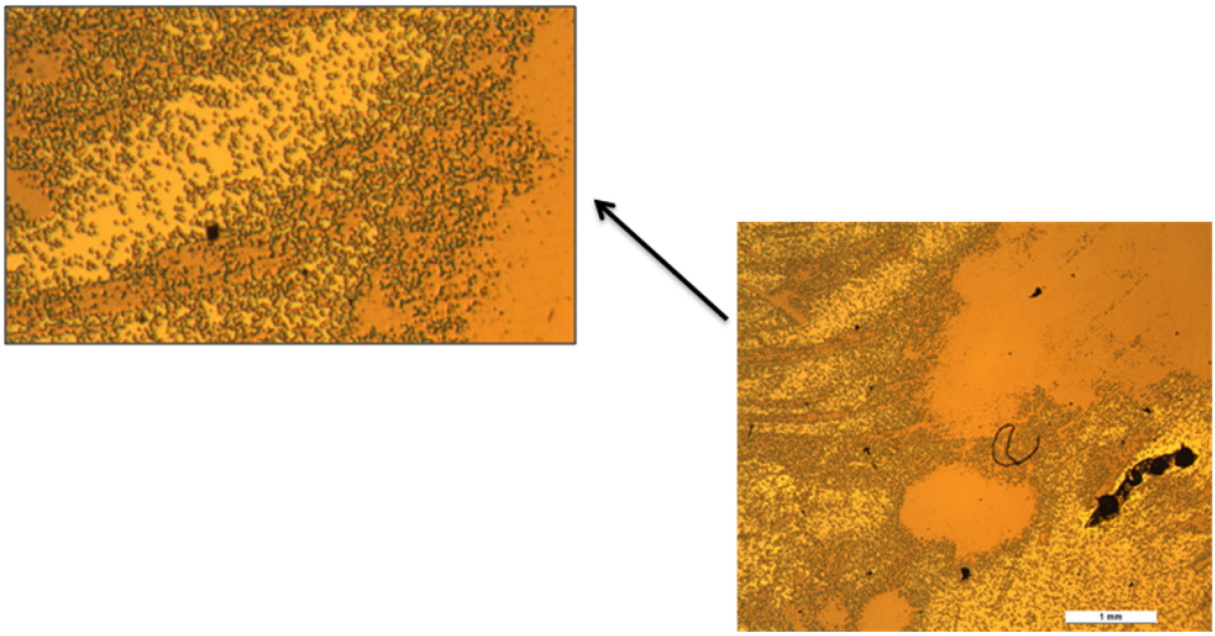


Fig. 3.101 Light optical micrograph of a 15.6 nm sSOI, decorated with 100 ppm Cu, etched with OPE F; residual layer thickness: 8.9 nm. The very high density of dark spots is due to artefact formation. Magnified view on the left side to illustrate the high density of artefacts.

Fig. 3.102 outlines the defect densities obtained for Ref 1 and copper-decorated samples. Copper decoration caused a significant increase in the DD compared to the DD of the reference. At copper concentrations from 0.01 to 1 ppm the DD increased continuously. However, at a copper concentration of 10 ppm the DD decreased unexpectedly to much lower values. No clear relationship between copper concentration and defect density could be observed for the copper concentration of 100 ppm due to the high artefact formation caused by copper precipitation.

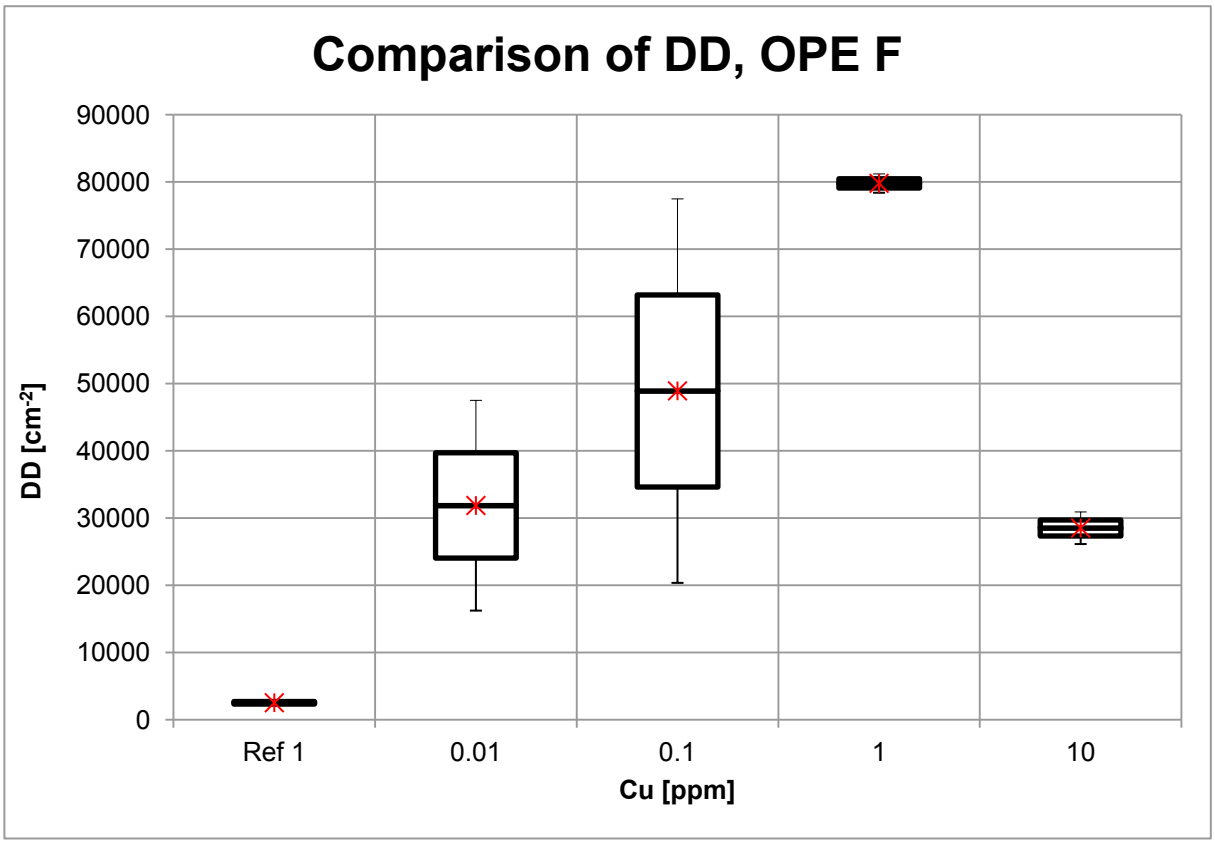


Fig. 3.102 of Ref 1 and Cu decorated 15.6 nm sSOI samples.

Conclusion

The OPE F etching solution was also not able to reveal stacking faults in copper decorated sSOI samples. A copper concentration of 0.01–1 ppm resulted in a steady increase in DD of TD attributable to the decoration procedure. At a copper concentration of 100 ppm artefact formation was too high for any reasonable determination of defect density.

3.10.5 OPE B

At an initial sSOI layer thickness of 15.6 nm delamination of the sSOI film was observed after copper decoration when OPE B was used as the etching solution. For this reason a thicker sSOI-film of about 83.5 nm was used while the BOX thickness was approx. 145 nm.

Copper decoration was accomplished by furnace annealing. More copper concentrations could be tested in these studies due to the availability of the 83.5 nm sSOI fragments. A volume of 0.5-1.5 µL of $Cu(NO_3)_2$ solution with copper concentrations ranging from 0.0001-100 ppm was applied on the back of several sSOI fragments and dried by heating on a hot plate. The fragments were then annealed mainly at 800 °C for 1 min in a furnace. A few sSOI fragments were annealed at 860 °C to study the influence of a higher annealing temperature

on the defect delineation. The fragments were then quenched in air to room temperature. Some of the sSOI fragments were etched with dilute Secco (0.04 M Cr (VI)) from their initial layer thickness of 83.5 nm down to approx. 30 nm and treated with a dip in HF for approx. 23 s to reveal the defects, primarily stacking faults (SF) and threading dislocations (TD) [122].

The results were compared to those of:

a) Non-decorated OPE B etched fragments (“OPE B-reference”) and
b) Decorated and non-decorated dilute Secco etched fragments (“dil. Secco-reference”)

Optical micrographs of Secco etched samples with and without copper decoration display a high density of stacking faults (SF) and threading dislocations (TD) albeit in sSOI samples of an early stage in the development of this material (Fig. 3.103).

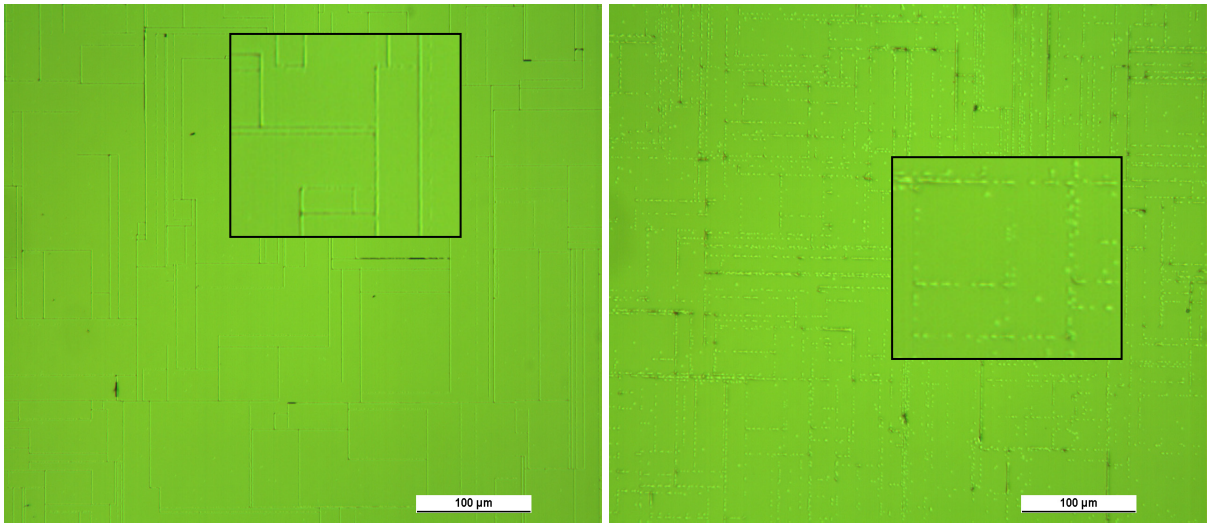


Fig. 3.103 Left: Light optical micrograph of an 83.5 nm Ref 1 sSOI sample, etched with dilute Secco (0.04 M Cr(VI)) for 54 s; residual layer thickness: 28 nm.
Right: Light optical micrograph of an 83.5 nm sSOI sample, decorated with 0.75 µL of a 10 ppm $Cu(NO_3)_2$ solution, etched with dilute Secco (0.04 M Cr (VI)) for 54 s; residual layer thickness: 25 nm.

With OPE B solution a few bright dots were revealed on non-copper decorated samples which correspond to the halos produced by an etched BOX at the TD etch pit (Fig. 3.104). A few TD were revealed but not SF.

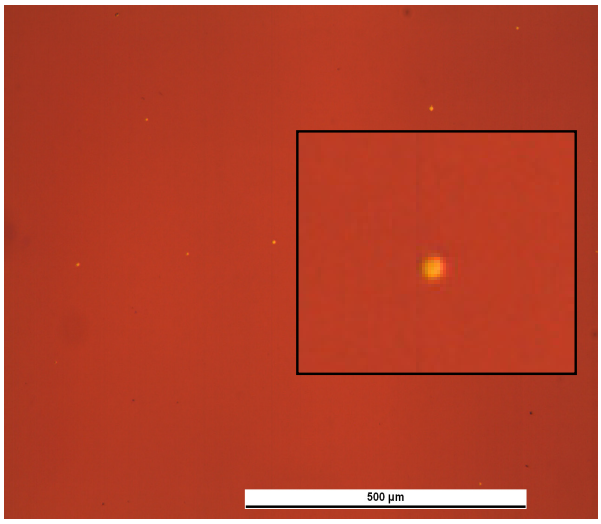


Fig. 3.104 Light optical micrograph of an 83.5 nm Ref 1 sSOI sample, etched with OPE B for 14 min; residual layer thickness: 58 nm.

A sSOI fragment decorated with 0.1 ppm Cu and etched with an OPE B solution can be seen in Fig. 3.105. The density of dots is much higher than that of the reference. There is a suspicion of SF but no definite traces.

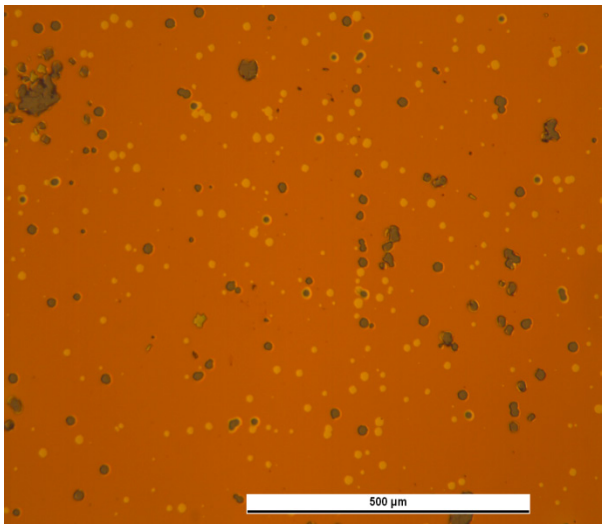


Fig. 3.105 Light optical micrograph of an 83.5 nm sSOI sample, decorated with 0.5 µL of a 0.1 ppm $Cu(NO_3)_2$ solution, annealed at 800 °C, etched with OPE B for 22.5 min; residual layer thickness: 52 nm.

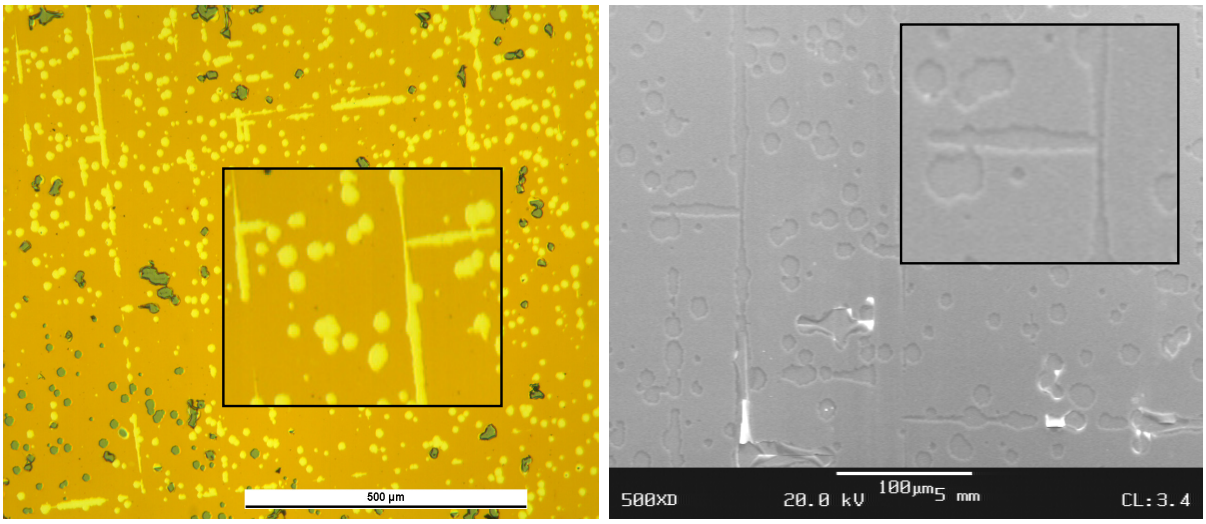


Fig. 3.106 Light optical micrograph (left) and SEM (right) of an 83.5 nm sSOI sample, decorated with 0.5 µL of a 10 ppm $Cu(NO_3)_2$ solution, annealed at 800 °C; etched with OPE B; residual layer thickness: 48 nm.

sSOI fragments were decorated with 10 ppm copper and subsequently etched with OPE B solution (Fig. 3.106). The images show dots which may correspond to TDs and arrays of dots and lines which may be attributed to SF.

The OPE B solution proved to be the best OPE etching solution for copper decorated fragments. The experimental parameters for copper decoration via furnace annealing were determined. The best results were achieved with 0.5 and 0.75 µL (no difference was observed between both volumes) of a 10 ppm $Cu(NO_3)_2$ solution deposited on the back of the sSOI fragment. A furnace annealing temperature of 800 °C was found to be suitable; a higher annealing temperature (860 °C) resulted in a lower density of SF. Compared to the samples etched with dilute Secco in which the residual layer thickness was 25 to 30 nm (about 60% removed), with OPE B, at a residual layer thickness of 45–50 nm (30-40% removed) both stacking faults and threading dislocations were revealed.

In Fig. 3.107 and Fig. 3.108 further examples of samples decorated with 10 ppm Cu and etched with OPE B are shown. The desired improvement of SF delineation was achieved by the experimental conditions described. Single bright and dark dots as well as arrays of dots are displayed which very likely correspond to TDs (dots) and SF (arrays of dots and occasionally even lines).

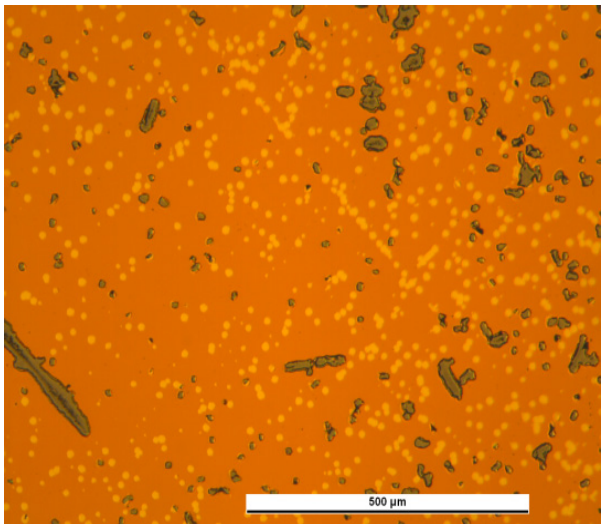


Fig. 3.107 Light optical micrograph of an 83.5 nm sSOI sample, decorated with 0.5 µL of 10 ppm of $Cu(NO_3)_2$ solution, annealed at 800 °C; etched with OPE B; not dipped in HF; residual layer thickness: 48 nm.

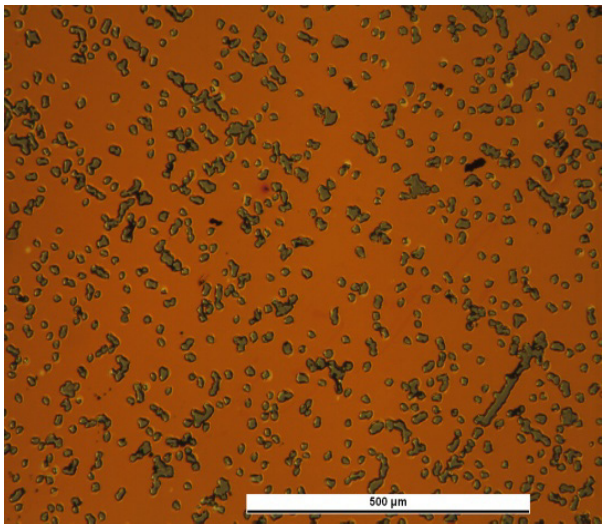


Fig. 3.108 Light optical micrograph of an 83.5 nm sSOI sample, decorated with 0.5 µL of a 10 ppm $Cu(NO_3)_2$ solution, annealed at 800 °C; etched with OPE B; not dipped in HF; residual layer thickness: 50 nm.

Some sSOI fragments were copper decorated with a copper concentration of 100 ppm and subsequently etched with OPE B (Fig. 3.109). A very high density of dots was obtained caused by artefact formation. The high copper concentration resulted in a surface covered with dots, of which a large part are Cu precipitates (artefacts) on the surface.

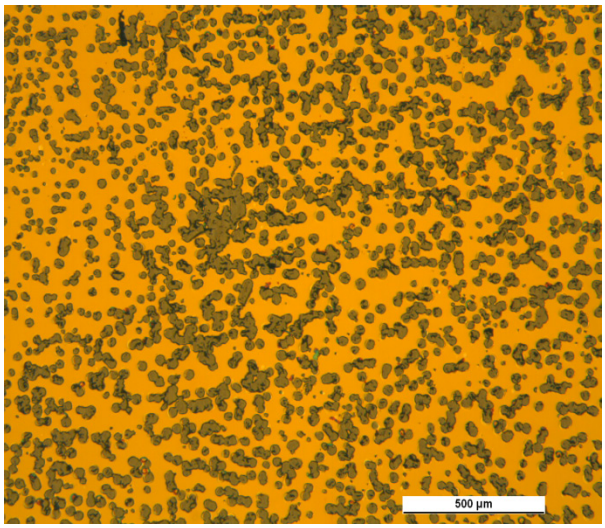


Fig. 3.109 Light optical micrograph of an 83.5 nm sSOI sample, decorated with 0.5 µL of a 100 ppm $Cu(NO_3)_2$ solution, annealed at 800 °C; etched with OPE B; not dipped in HF; high artefact formation.

Tab. 3.16 shows both the experimental conditions and the optimized parameters to provide an overview of the results obtained.

Tab. 3.16 Experimental conditions and the results obtained to reveal both TD and SF in sSOI.

Experimental parameter tested	**optimized conditions**
0.5-1.5 µL of 0.0001-100 ppm Cu	0.5-0.75 µL of 10 ppm Cu
Annealing temp.: 800-860 °C	Annealing temp.: 800 °C
OPE A/B/C/D/F	OPE B
Residual LT analysed: 37-65 nm	Residual LT: 45-50 nm (OPE B) (vs. dilute Secco: 25-30 nm)

Conclusion:

The OPE B solution proved to be the best etching solution for a combination of copper decoration and etching for the delineation of both stacking faults and threading dislocations in sSOI. The experimental conditions were developed and optimized. The best results were obtained using a copper concentration of 10 ppm and an annealing temperature of 800 °C. Etching down to a residual layer thickness of 45 to 50 nm leads to the best delineation of both defect types TD and SF.

TD result in a more pronounced distorted lattice compared to SF and are therefore the preferred choice as nucleation sites. Therefore, a low copper concentration yields a decoration of TD only. With SF the strain in the lattice is much weaker, hence, a much higher copper concentration is needed for copper precipitation.

3.11 Influence of metal decoration on the defect etching process

Parameters such as removal rate, selectivity and activation energy for the etching process were used to describe and characterise the influence of metal decoration on preferential etching of defects in SOI wafers [123]. The selectivity of the dilute Secco etch (0.04 M Cr (VI)) was determined experimentally on dislocations generated by damaging silicon substrates by indentation with a diamond tip and subsequent annealing at 1 000 °C. After dilute Secco etching the depth of the dislocation etch pits was measured by an atomic force microscope (AFM). The selectivity and the activation energy of non-decorated samples were compared with those of copper and lithium decorated samples.

At a crystal defect the removal rate should increase due to a decrease in activation energy for the etching process. The increased removal rate causes the formation of pits. The depth of these pits can be measured by AFM. The depth of an etch pit is affected by the selectivity [116] of the attack on the crystal defect. The higher the selectivity of an etching solution the deeper the etch pit should be. The selectivity S describes the ratio of the removal at the crystal defect and the removal at the perfect crystal.

$$\mathbf{S = selectivity} = \frac{\mathbf{removal_{perfect\ material} + depth_{etch\ pit}}}{\mathbf{removal_{perfect\ material}}} = \frac{\mathbf{removal_{crystal\ defect}}}{\mathbf{removal_{perfect\ material}}}$$

3.11.1 Determination of activation energies of defect etching with a dilute Secco etch (0.04 M Cr (VI))

The potential energy of the lattice is increased at a crystal defect and, hence, the activation energy for the etching process is reduced and consequently the removal rate is enhanced. The decreased activation energy can be determined by the Arrhenius equation:

$$\ln(r) = \ln(A) - \frac{E_a}{RT}$$

$$E_a = (\ln(A) - \ln(r)\, RT$$

where

E_a	activation energy of the etching process of silicon
ln r	logarithm of the removal rate at the defect (25 °C)
R	2.479 kJ/mol
T	298.15 K

A pre-exponential factor, determined experimentally

The activation energies were determined for the preferential etching process using a dilute Secco etch (0.04 M Cr (VI)) on non-decorated references and Cu or Li decorated samples of SOI material. A third type of reference sample was Ref 3, which was annealed without decoration in the quartz tube, and then Secco etched.

The material used had a SOI layer thickness of 88 nm and a BOX thickness of 145 nm. Decoration was accomplished by depositing dilute $Cu(NO_3)_2$ and $LiNO_3$ solutions with concentrations of Cu or Li in the range 0.0001-10 ppm on the back of the sample, followed by drying and annealing the samples at 800 °C (see section 3.1). Six different etching temperatures (-2 °C, 3 °C, 8 °C, 13 °C, 18 °C and 23 °C) were used for the determination of the etch rates of the dilute Secco etch of the references and of each [Cu]. The removal of the SOI layer was measured by ellipsometry after etching. The overall activation energy for the etching process was evaluated via an Arrhenius plot of the etch rate as a function of temperature.

Tab. 3.17 Activation energies Ea of Ref 1, Ref 2 and Cu decorated samples.

Cu [ppm]	E_a [kJ/mol]
Ref 1	29.10
Ref 2	30.30
0.0001	30.82
0.001	29.77
0.01	29.58
0.1	32.22
1	29.72
10	30.02

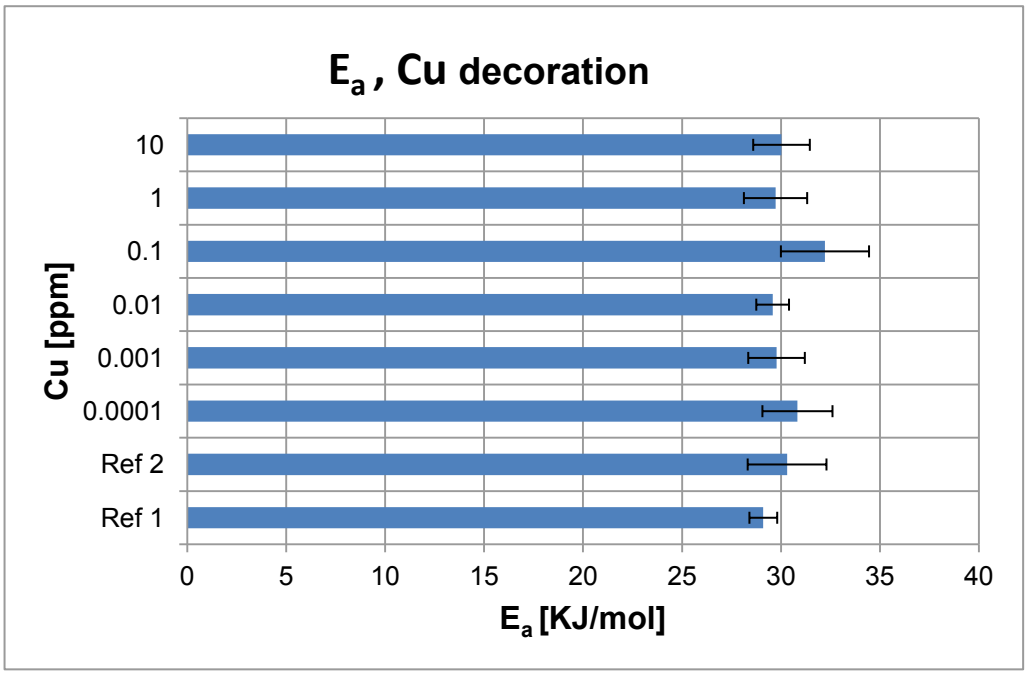


Fig. 3.110 Diagram of activation energies of Ref 1, Ref 2 and Cu decorated samples.

Tab. 3.18 Activation energies Ea of Ref 1, Ref 3 and Li decorated samples.

Li [ppm]	E_a [kJ/mol]
Ref 1	29.10
Ref 3	33.18
0.0001	33.94
0.001	28.79
0.01	31.50
0.1	30.60
1	33.10
10	31.69

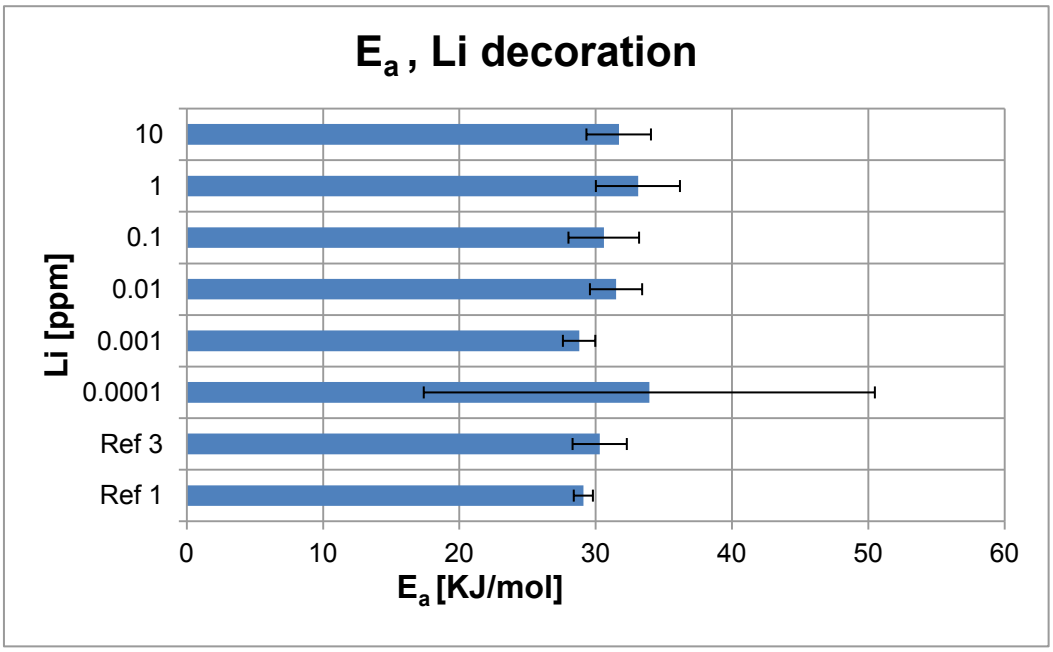


Fig. 3.111 Diagram of activation energies of Ref 1, Ref 3 and Li decorated samples.

Fig. 3.110 and Fig. 3.111 and Tab. 3.17 and Tab. 3.18 show the results of the activation energies obtained for Ref 1–3, copper and lithium decorated samples of SOI. The activation energies of the copper decorated samples range from 29.6 to 32.2 kJ/mol, but do not exhibit any relationship to Cu concentration. In the case of lithium the values range from 28.8 to 33.9 kJ/mol. Here again there is no relationship between lithium concentration and activation energy. Similar values for the activation energies were obtained for the reference samples (Ref 1: 29.1 kJ/mol, Ref 2: 30.3 kJ/mol, Ref.3 33,2 kJ/mol).

Interpretation and conclusion

The samples used had low or moderate defect densities. To determine the removal rate, the thickness of the SOI film remaining after etching was determined using an ellipsometer which measured the thickness of the film at various points in the sample and did not necessarily include an etch pit. As the defect densities were low, the probability of measuring the thickness at an etch pit was low. Therefore between decorated and non-decorated samples a significant difference in activation energies was neither expected nor observed (Fig. 3.110 and Fig. 3.111).

3.11.2 Determination of the selectivity of a dilute Secco etch (0.04 M Cr (VI)) in the delineation of dislocations with and without metal decoration

The selectivity of the dilute Secco etch (0.04 M Cr (VI)) was determined experimentally on dislocations in copper and lithium decorated and non-decorated Ref 1 Czochralski (CZ) silicon bulk fragments (size: approx. 1 square cm). The physical and chemical properties of the silicon bulk used are given in Tab. 3.19.

Tab. 3.19 Physical and chemical properties of the Si-Bulk.

Material	Thickness [µm]	Diameter [mm]	Orientation	Dopant/Resistivity [Ωcm]
CZ-bulk Supplier 1	750	300	(100)	p-doped 20-25

Dislocations were generated by damaging the silicon samples by indentation with a diamond tip (four indentations were made in the centre of each sample) and subsequent annealing at 1 000 °C under argon atmosphere in a RTP (Rapid Thermal Processing) system. In the annealing process the mechanical stress in the damaged crystal lattice is relaxed by the generation of dislocation half-loops.

Some of the samples were then decorated using dilute $Cu(NO_3)_2$ and $LiNO_3$ solutions (0.0001, 0.1, 1 and 10 ppm of Cu or Li) as described earlier. The decorated and non-decorated samples were then etched with dilute Secco etch (0.04 M Cr (VI)) at room temperature using different etching times (3-5 min). After preferential etching the depths of the dislocation etch pits were measured by an atomic force microscope (AFM). The selectivity S of the etching process is determined as the ratio of the removal at the crystal defect (dislocation) and the removal at the perfect crystal. The removal at the dislocation is given by the overall removal of the perfect crystal plus the depth of the dislocation etch pit.

Preferential etching solutions are capable of differentiating between local levels of the potential energy in the perfect silicon lattice. In principle two main factors contribute to the increase of the potential energy at a dislocation:

- The strain field produced by distorted bonds of the atoms at the dislocation core and
- Impurities, in particular metals, segregated to the dislocation due to an intentional decoration procedure

For the etching reaction at the perfect lattice the energy barrier E_a is much higher than at the dislocation. Hence, etch rates at dislocations are higher than etch rates of the perfect lattice

giving rise to the formation of etch pits at dislocations where they emerge at the crystal surface. Moreover, metal silicide precipitates themselves, formed in a decoration procedure at defects such as dislocations, provide a reaction path with a reduced energy barrier resulting in a drastic increase of the etch rate.

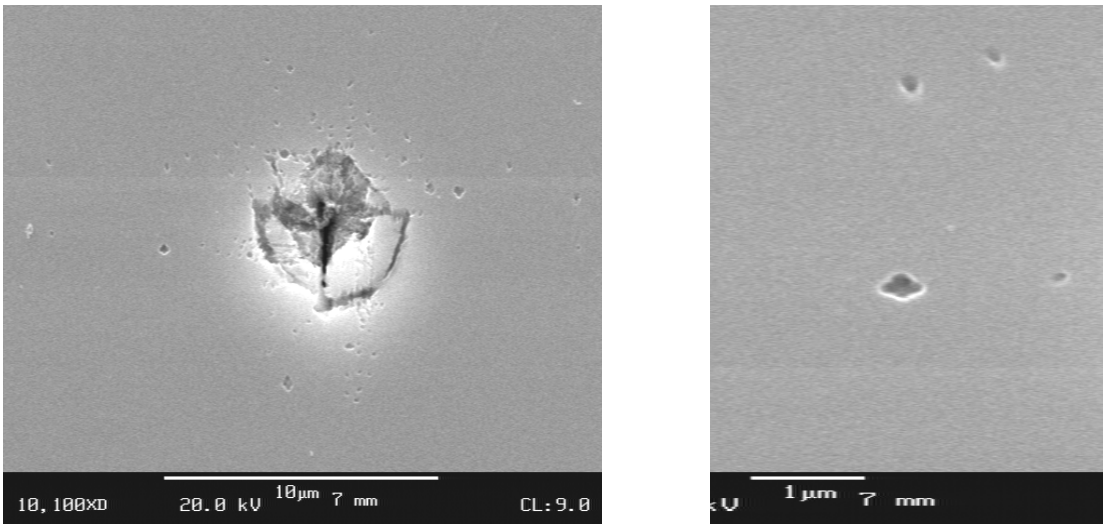


Fig. 3.112 SEM images of dislocation etch pits (left). Magnified view of non-decorated dislocations (right). Indentation with non-decorated dislocation half loops generated during annealing at 1 000 °C.

Fig. 3.112, Fig. 3.113 and Fig. 3.114 display scanning electron micrographs (SEM) of indentations (left images) after annealing without decoration (Fig. 3.112, left), with 0.1 ppm Cu (Fig. 3.113, left) and with 0.1 ppm Li decoration (Fig. 3.114, left) and dislocation etch pits of non-decorated (Fig. 3.112, right), Cu decorated (Fig. 3.113, right) and Li decorated (Fig. 3.114, right) samples.

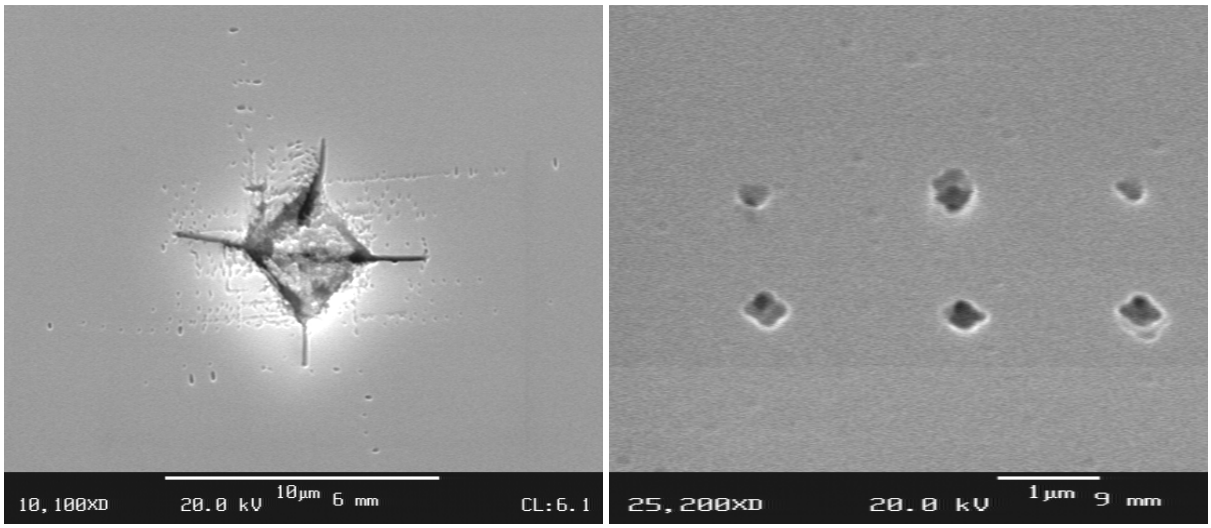


Fig. 3.113 SEM images of Cu decorated dislocation etch pits (left). Magnified view of the dislocations (right). Indentation with 0.1 ppm Cu decorated dislocation half loops generated during annealing at 1 000 °C.

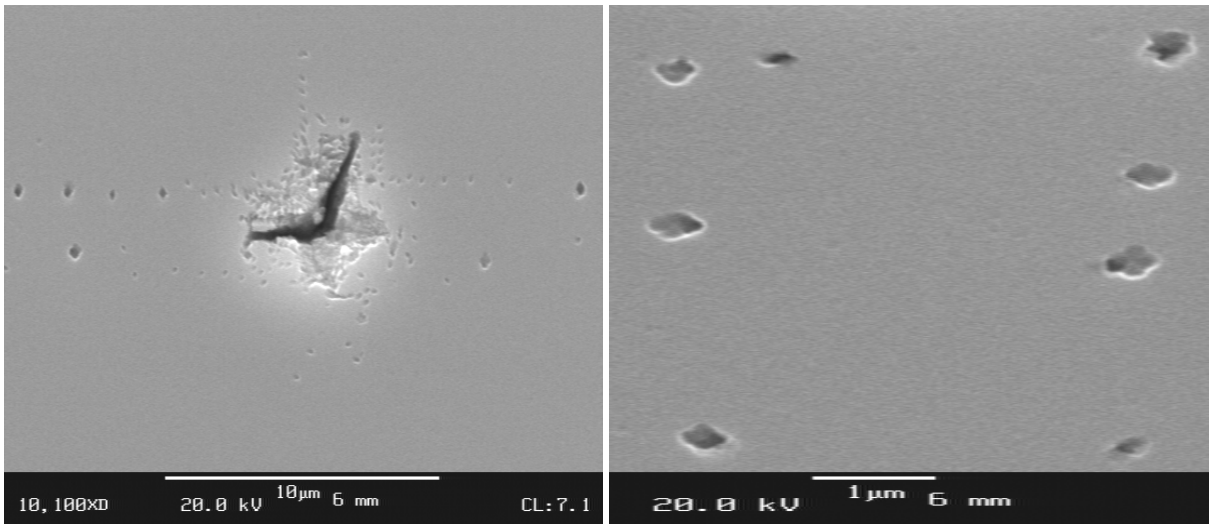


Fig. 3.114 SEM images of Li decorated dislocation etch pits (left). Magnified view of the dislocations (right). Indentation with 0.1 ppm Li decorated dislocation half loops generated during annealing at 1 000 °C.

The depth of dislocation etch pits on reference and copper and lithium decorated samples were measured after a dilute Secco etch with an atomic force microscope (AFM).

A cantilever tip consisting of silicon with a height of 11 µm and a diameter of approximately 10 nm was used for these AFM analyses. Both the tip angle α and the diameter of the etch pit determine the maximum depth that can be measured via AFM. The tip angle lies between 10° and 25°.

In this case the depth of dislocation half loops is calculated. The maximum determinable depth of the etch pit of a dislocation half loop depends on the etching time used (Fig. 3.115):

- *Increased etching time:*
  The etching solution preferentially enlarges the etch pits in a lateral direction. The diameter of the pits increases and their shape appears shallower. The tip cannot get to the deepest point of the pit, in which case the calculated depth will be too low. Therefore, the selectivities determined are not reliable.

- *Short etching time:*
  The AFM tip should be able to reach the bottom of the etch pit, hence, the measured depth should be more reliable.

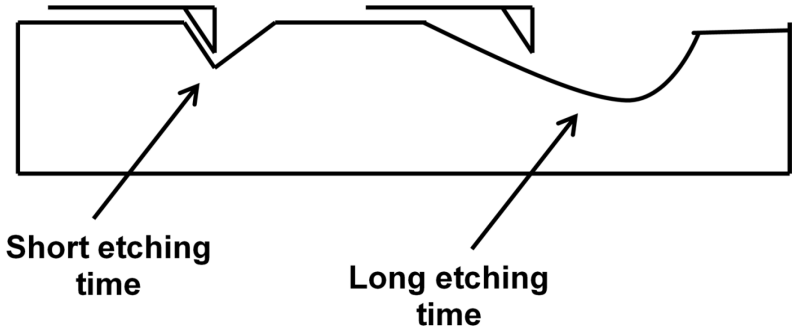


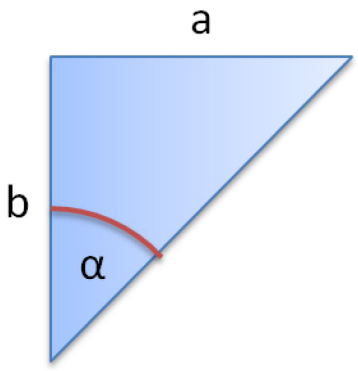
Fig. 3.115 The maximum determinable depth of an etch pit by an AFM is dependent on:

a) geometry of the etch pit.
b) depth of the etch pit.

The following equation can be used to evaluate the possible *maximum depth of an etch pit:*

$$\tan(\alpha) = \frac{a}{b}$$

$$b = \frac{a}{\tan(\alpha)}$$



where

a diameter of the etch pit

b the maximum depth and

α tip angle

Fig. 3.116-Fig. 3.120 show typical section analyses for the determination of depth of Ref 1, Cu and Li decorated silicon bulk samples. Several fragments were used for each metal concentration (0.0001, 0.1, 1 and 10 ppm of Cu or Li) and for the references to obtain an average value for the selectivities.

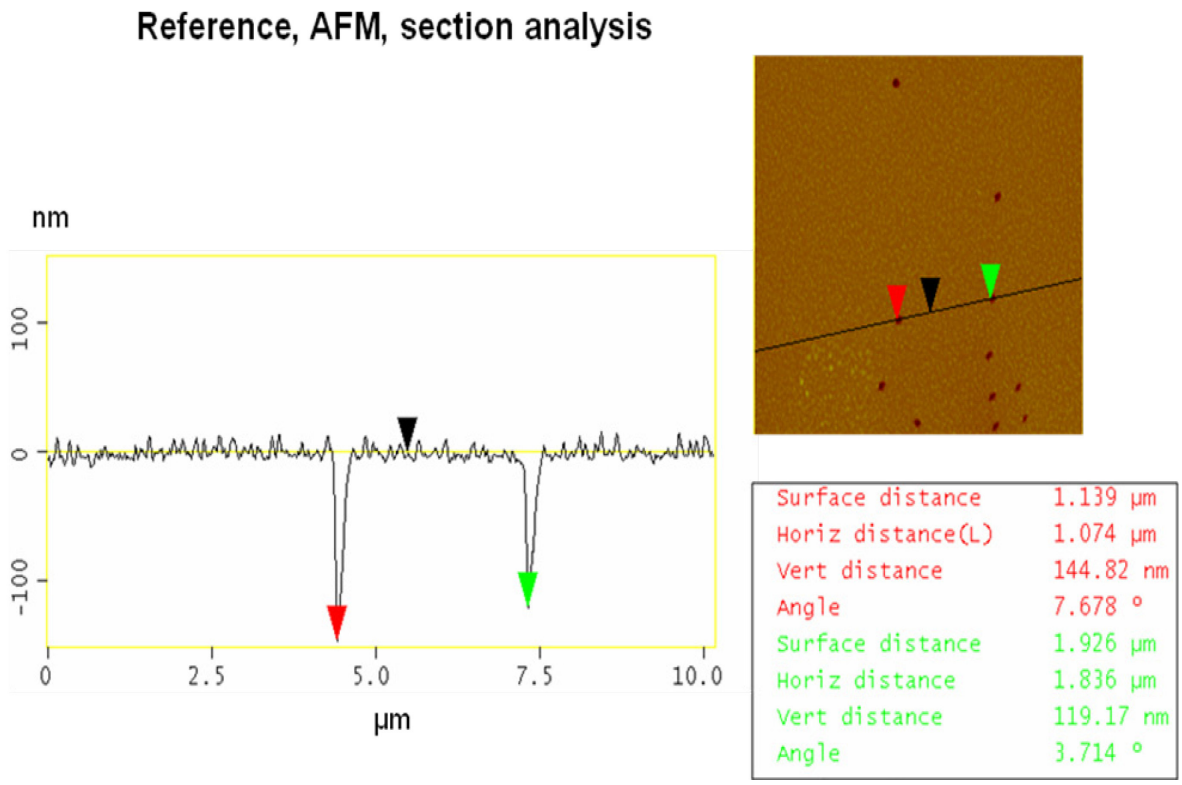


Fig. 3.116 AFM image of two etch pits (insert) of a Ref 1 sample and measurement of etch pit depth by section analysis (line scan).

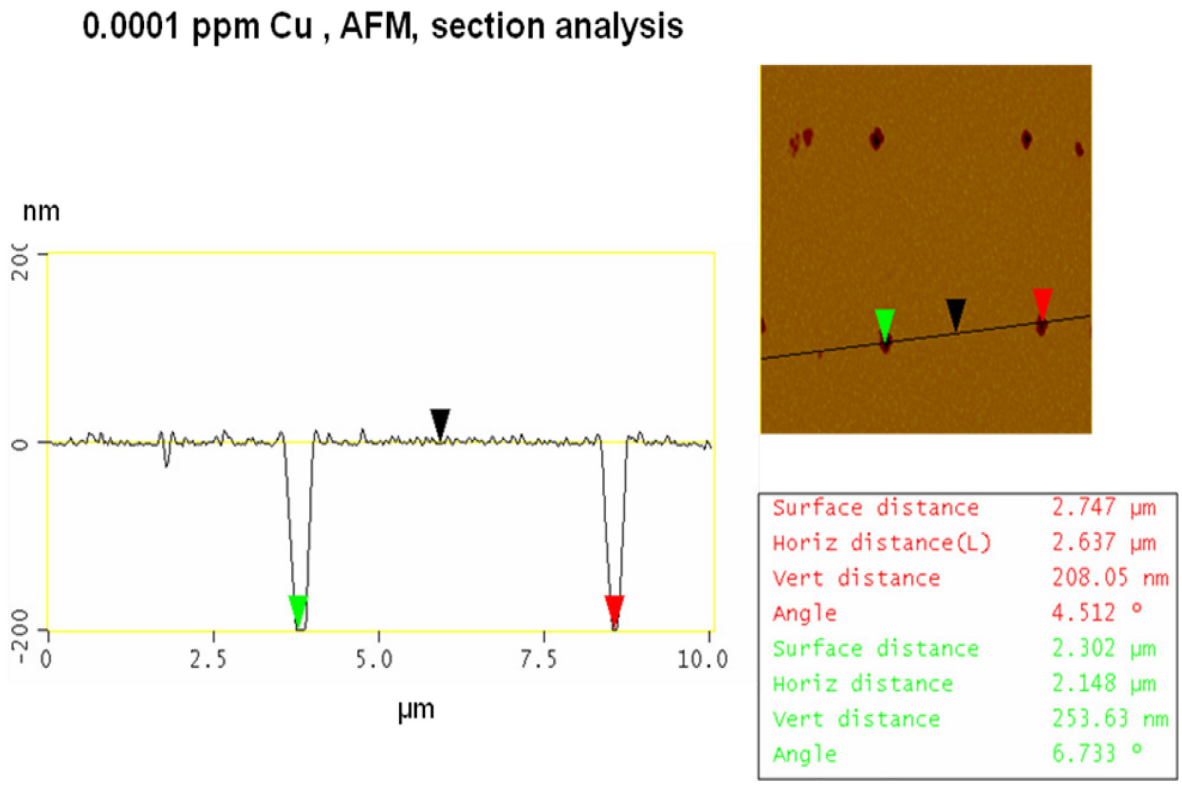


Fig. 3.117 Sample decorated with 0.0001 ppm Cu; AFM image of two etch pits (insert) and measurement of etch pit depth by section analysis (line scan).

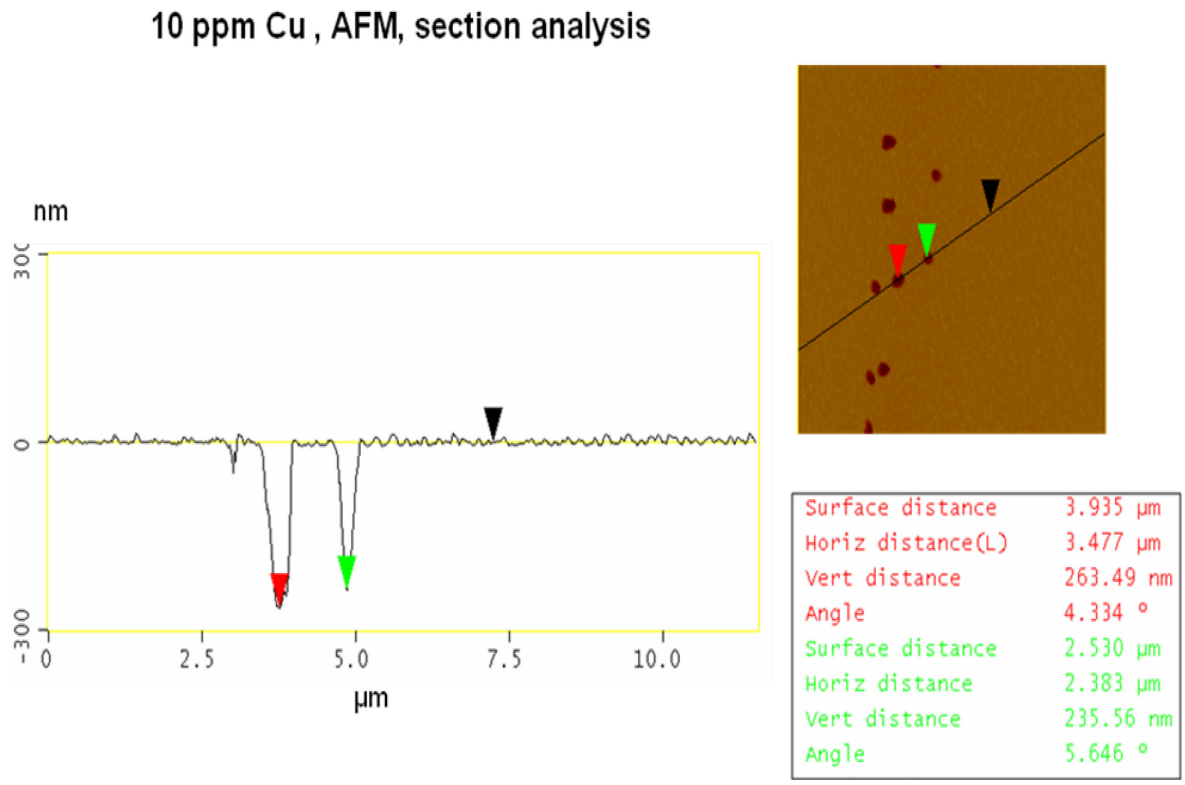


Fig. 3.118 AFM image of two etch pits (insert) of a sample decorated with 10 ppm Cu and measurement of etch pit depth by section analysis (line scan).

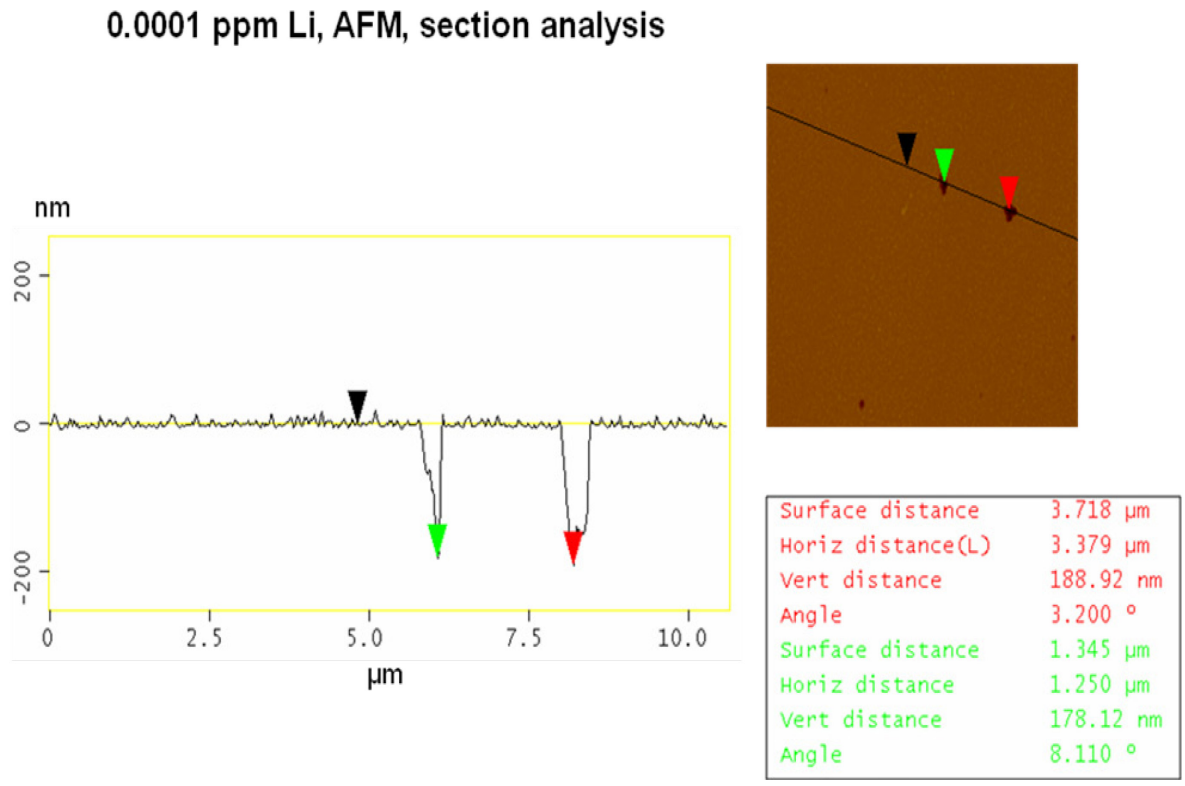


Fig. 3.119 Sample decorated with 0.0001 ppm Li; AFM image of two etch pits (insert) and measurement of etch pit depth by section analysis (line scan).

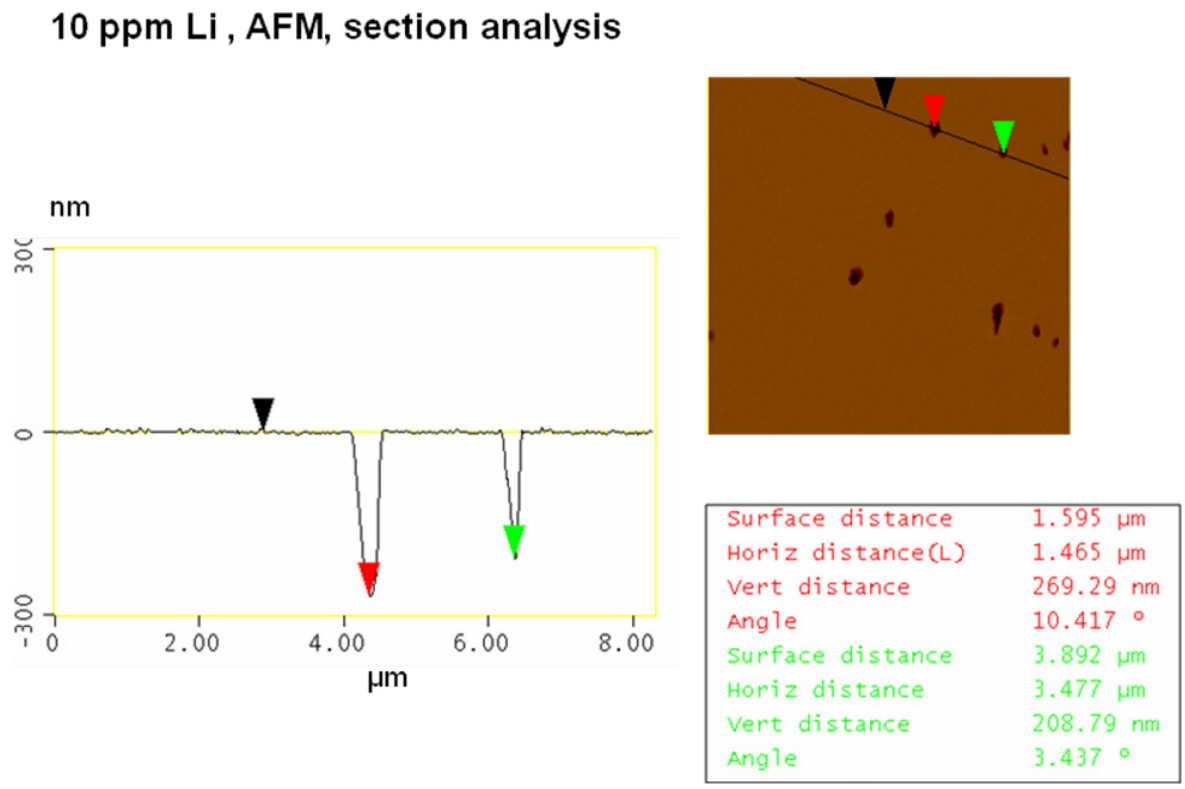


Fig. 3.120 AFM image of two etch pits (insert) of a sample decorated with 10 ppm Li and measurement of etch pit depth by section analysis (line scan).

The selectivities were calculated according to the equation defined for the determination of selectivity (Tab. 3.20 and Tab. 3.21) and plotted in Fig. 3.121. Decoration resulted in an increase of the selectivity over the reference of 13-53% for copper and 10-29% for lithium. 10 ppm of copper yielded the highest increase in selectivity (53%).

Tab. 3.20 S of Ref 1 and Cu decorated samples.

Cu [ppm]	S	Increase [%]
Ref 1	1.95	-
0.0001	2.25	16
0.1	2.22	14
1	2.19	13
10	3.00	53

Tab. 3.21 Selectivities S of Ref 1 and Li decorated samples.

Li [ppm]	S	Increase [%]
Ref 1	1.95	-
0.0001	2.14	10
0.1	2.23	15
1	2.14	10
10	2.50	29

The value for the Ref 1 samples was about 1.95 and increased using copper and lithium decoration up to 2.14-3.0 (10-53% increase).

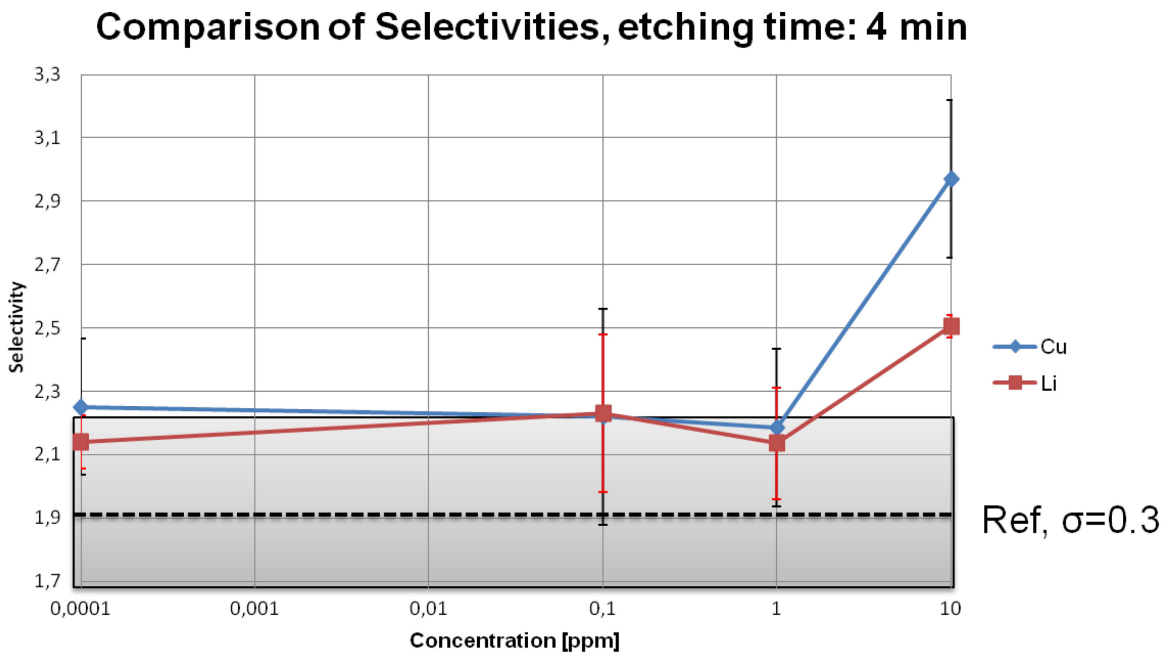


Fig. 3.121 Comparison of the selectivities of Ref 1 and Cu and Li decorated samples.

Interpretation and conclusion

As expected the selectivity of the dilute Secco etch (0.04 M Cr (VI)) was lowest for the dislocations in the non-decorated samples. The value of 1.95 is in good agreement with a value of about 1.8 obtained in similar experiments with dilute Secco etch (0.04 M Cr (VI)) performed by D. Possner [112, 116]. After copper decoration of the dislocations the

selectivity increased moderately but remained at nearly the same level in the samples decorated with 0.0001 to 1 ppm copper. Since in the experiment only a few dislocation half-loops had been generated at the indentations even at the low copper levels the amount of copper available was sufficient to decorate these dislocations. At the 10 ppm Cu level the degree of copper precipitation and Cu-silicide formation at the dislocations had to be extremely high. Here the etching behaviour is dominated by the Cu-silicide resulting in this extraordinary high selectivity value of about 3. In the case of lithium the behaviour of the samples is similar. In measurements by secondary ion mass spectrometry some cross-contamination by copper, originating, e.g., during annealing in the furnace, was detected on such samples. The sharp increase in selectivity of the lithium decorated samples may be partly due to this effect.

4 Summary

Silicon wafers such as Silicon on Insulator (SOI) and strained silicon on Insulator (sSOI) are the essential and basic materials of advanced microelectronic devices. However, they often show various kinds of crystal defects which impair the function of these devices. The most efficient method to date, for detecting such defects and for determining their density, is to delineate them by etching the wafers with a suitable etching solution and characterise them via light optical microscopy. Etch pits are formed at defect sites which are etched at a faster rate than at the perfect lattice. The standard etching solution used for SOI and sSOI is a dilute version of Secco. As Secco contains carcinogenic and environmentally hazardous chromium (VI), the use of which is or will be restricted by law in many countries, suitable chromium (VI)-free etching solutions like Organic Peracid Etches (OPE), modified Chemical Polishing Etches (CP) like CP4 mod and mixtures with organic oxidizing agents like chloranil (CA) have been developed for the successful delineation of various types of crystal defects.

However there are still nanometer-sized defects which are hard to detect or escape detection by this method. Copper decoration is a well known method to magnify these defects. It consists in applying a copper nitrate solution to the back of the SOI or sSOI wafer. On annealing, copper diffuses through the substrate and the BOX (buried oxide) to the SOI/sSOI film and on quenching to room temperature, copper precipitates as copper silicide, $SiCu_3$, foremost at crystal defects where the lattice strain is greater than at perfect lattice sites. These silicides increase the volume in these parts of the crystal lattice and defect magnification occurs. A considerable disadvantage of this method is its tendency for artefact formation, when the copper concentration used is too high, with the copper precipitating at the film surface. The consequence is a higher density of etch pits whereby true defect etch pits cannot be differentiated from those caused by artefacts.

The aim of this thesis is to show that the processes of decorating and etching can be combined successfully to delineate all crystal defects in SOI and sSOI. An ideal result would have been to find a copper decoration procedure that decorates all existing crystal defects at a copper concentration that avoids artefact formation.

The SOI and sSOI layers on wafers used for the experiments had thicknesses ranging from 60-1 400 nm and 14-84 nm respectively. The defects delineated were so-called Crystal-originated Particles (COPs) (vacancy agglomerates), “Red Spots” and oxidation induced stacking faults (OiSF) in SOI and process induced stacking faults (SF) and threading dislocations (TD) in sSOI. Two types of defect features could be delineated in thick SOI: defects with and defects without a halo. Defects with a halo may originate from the upper

part of the SOI film giving rise to etch pits which protrude down to the BOX and produce a halo by etching the BOX during the dip in HF. Defects without a halo may be located in the deeper parts of the SOI film producing etch pits which do not reach the BOX. Therefore no underetching of the BOX takes place during the HF dip.

Dilute Secco (0.04 M Cr (VI)) was used as standard etching solution both for SOI and sSOI. The chromium-free alternatives tested were OPE on SOI and sSOI, CP4 on 610 nm SOI, CA on standard SOI and Jeita on 1 400 nm SOI. Jeita A and B are two alternative solutions which were used for etching especially thick SOI because of their higher etching rates. Jeita A contains HNO_3, HF and HAc, Jeita B contains additionally KI. In all cases, the results were compared with those obtained with dilute Secco. The main criteria for the choice of etching solution were the thickness of the SOI/sSOI film and the results obtained previously for non-decorated delineation by others in the field. The etching time was determined by both the thickness of the film and the etch rate of the solution used.

Reference samples, where necessary, were both non-decorated and non-annealed etched samples (Ref 1) and non-decorated but annealed and etched samples (Ref 2). Copper decorated samples were compared to both references in respect of defect density (DD) and defect characterisation, which were determined using a light optical microscope, an atomic force microscope (AFM) and a scanning electron microscope (SEM).

In order to bypass the problem of artefact formation during the annealing process in the furnace an attempt was made to copper decorate the SOI and sSOI films by electrochemical deposition out of a dilute $Cu(NO_3)_2$ spiked hydrofluoric acid solution, followed by etching with dilute Secco. The result was the nucleation and growth of copper particles on the sample surface and hence, a much higher density of etch pits compared to the typical values obtained for furnace annealed samples. This method was unsuitable for the determination of COPs in SOI but good results were obtained for stacking faults and threading dislocations in sSOI after decoration with a 0.1 ppm copper spiked solution.

Copper decoration via furnace annealing was therefore used as the standard decoration procedure on different SOI wafers with different layer thicknesses and the experimental parameters were improved and refined to suit each sample type. For defect delineation in standard SOI with layer thicknesses of 60-149 nm several chromium-free etching solutions were used in addition to the dilute Secco.

OPE D, used to etch copper decorated standard SOI, produced pits with much larger radii than those produced with dilute Secco. OPE D has a comparatively low etch rate, and the longer etching times hence required resulted in larger etch pits close to the surface and

smaller ones deeper in the SOI film. The defect densities obtained with OPE D etched samples were also consistently higher.

Defect densities of process induced OiSF in 90 nm SOI wafers were also determined with a view to reducing their occurrence during their production. Chromium-free chloranil (2,3,5,6-tetrachloro-1,4-benzoquinone) was compared with dilute Secco for its efficiency in delineating OiSFs in such samples. These experiments showed that the effects of copper decoration become visible at concentrations at and above 0.01 ppm of copper for both etchants. Copper decoration at these copper concentrations led to an improved detection of OiSF etched with the less sensitive CA solution. But the results did not attain the effectiveness of the dilute Secco which has a higher oxidizing potential.

Copper decoration experiments were also undertaken on thick SOI wafers (610 nm SOI, with 300 nm BOX and 1 400 nm SOI, with 1 000 nm BOX) to verify the feasibility and optimize the parameters of the procedure for thick SOI. Both sample types have very thick BOX layers which could act as a diffusion barrier for copper. However, at 900°C for the 300 nm BOX and 950 °C for the 1 000 nm BOX sufficient copper diffused through the BOX into the SOI layer and decorated the defects.

The 1 400 nm SOI samples were etched with a dilute Secco and the Jeita A and B etchants. Both the higher oxidizing potential and the higher selectivity of the dilute Secco led to a better delineation of defects with a halo while Jeita A and B produce a higher DD of small pits without a halo. The best copper concentration for delineating defects in 1 400 nm thick SOI appeared to be between 0.01 and 0.1 ppm with dilute Secco as the etching solution. No clear relationship was observed between copper concentration and defect densities for defects with and without a halo after etching with Jeita A or B. This could be due to their lower oxidizing potential and the lower selectivity.

SOI wafers with 610 nm SOI and 300 nm BOX were etched after copper decoration with CP4 + KIO_3 (CP4 A) and CP4 + KIO_3 + KI (CP4 B) and with dilute Secco (0.04 M Cr (VI)). With dilute Secco an increase in DD was observed at a [Cu] ≥ 0.1 ppm. The DD of Secco-etched samples were much higher than that obtained with CP4 A or CP4 B. With CP4 B no clear relationship could be established between copper concentration and DD. Neither CP4 A nor CP4 B was found to be a suitable substitute for dilute Secco.

For all the etching solutions tested, and sSOI and SOI layer thicknesses the optimal copper concentration for the decoration of different types of crystal defects was in the range of 0.01–0.1 ppm. At these concentrations a decoration effect of copper could be observed, while a

possible artefact formation could be largely avoided. In all cases, copper diffused through the BOX, the thickness of which ranged from 145 nm to 1 000 nm, and the annealing temperature was varied from 800–950 °C to adjust the BOX thickness.

Chromium-free OPE solutions were examined as an alternative to Secco etching for defect delineation in sSOI. Various OPE solutions were tested in conjunction with different copper concentrations to reveal not only threading dislocations but also stacking faults in sSOI. Here the OPE B solution proved to be the most suitable. The experimental conditions were developed and optimized in further tests.

Copper decoration and preferential etching tests were also conducted on 200 nm SIMOX samples with a BOX layer thickness of 95 nm from a batch of heavily scratched wafers. The crystal defects were COPs and, to a large extent, process-induced oxygen precipitates which occur close to the silicon film/BOX interface. The silicon film had therefore to be etched down much closer to the BOX than was the case with SOI. Copper decoration resulted in an increase in DD. The OPE B was used as chromium-free etching solution which produced DD comparable to that obtained with dilute Secco, making it a suitable alternative for less damaged SIMOX as well.

Lithium has been used successfully in the past to decorate silicon wafers [93] where it has been shown to produce little or no artefacts. In SOI and sSOI, however, lithium´s high affinity for oxygen could make diffusion through the BOX a problem. An attempt was made to decorate both standard SOI and a novel extra thin SOI (20 nm) with an ultra-thin BOX (10 nm) (ETSOI/UTBOXSOI) with lithium nitrate. As decoration experiments did not prove satisfactory and further experiments were beyond the scope of this study, attention was focused on the distribution of lithium over a vertical cross-section of the wafer to determine the extent of diffusion. While lithium passed easily through the ultra-thin BOX, in standard SOI the BOX (145 nm) proved to be a diffusion barrier. The results also suggest that vaporized lithium in the furnace entered directly the SOI film from the film surface.

The influence of metal decoration on preferential etching of crystal defects in standard SOI was rated in terms of the parameters removal rate, selectivity and activation energy for the etching process.

The selectivity of the dilute Secco etch was determined experimentally in copper and lithium decorated and non-decorated Czochralski (CZ) silicon bulk fragments. As expected the selectivity was lowest for dislocations in the reference samples. After decoration with 0.0001

to 1 ppm of copper or lithium the selectivity increased modestly. At the 10 ppm Cu level the degree of copper precipitation was extremely high.

There was no difference in removal rate between decorated and non-decorated SOI samples. The thickness of the SOI film remaining after etching was determined using an ellipsometer which measured the thickness of the film at various points on the sample surface. As the defect densities were low, the probability of measuring the thickness at an etch pit was low. Therefore, as expected, the activation energies were independent of the SOI thickness.

The successful development of decoration and preferential-etching methods leads to a much better delineation of crystal defects in SOI and sSOI semiconductor materials with different layer thicknesses.

5 Zusammenfassung

Silizium Wafer wie Silicon on Insulator (SOI) und strained Silicon on Insulator (sSOI) stellen die Basismaterialien für die mikroelektronischen Bauteile dar. Jedoch weisen sie oft verschiedene Arten von Kristalldefekten auf, welche die Funktionalität dieser Bauteile beeinflussen. Die effizienteste und bekannteste Methode, zum Nachweis solcher Kristalldefekte und für die Bestimmung ihrer Defektdichte, ist ihre Sichtbarmachung mittels Ätzen des Wafers mit einer geeigneten Ätzlösung. Die anschließende Charakterisierung erfolgt zunächst mit Hilfe der Lichtmikroskopie. Die Bildung von Ätzfiguren („etch pits“) an Defektstellen wird bedingt durch die schnellere Ätzrate am Defekt im Vergleich zum perfekten Kristallgitter. Die Standardätzlösung für SOI und sSOI ist eine verdünnte Version der Secco Lösung. Da die Secco krebserregendes und umweltschädigendes Chrom (VI) enthält, ist oder wird ihr Einsatz als Ätzlösung in immer mehr Ländern verboten. Geeignete Chrom (VI)-freie Ätzlösungen, wie die Organic Peracid Etches (OPE), modified Chemical Polishing Etches (CP) wie CP4 mod und Lösungen mit organischen oxidierenden Verbindungen wie Chloranil (CA), wurden für die erfolgreiche Sichtbarmachung verschiedener Arten an Kristalldefekten entwickelt.

Dennoch gibt es immer noch Kristalldefekt, welche eine Größe im nm-Bereich aufweisen, welche mit den erwähnten Ätzmethoden kaum oder nicht nachgewiesen werden können. Das bekannte Verfahren der Kupferdekoration wird für die Vergrößerung derartige Defekte eingesetzt. Dabei wird eine definierte Menge an Kupfernitrat auf die Rückseite des SOI bzw. sSOI Wafers aufgebracht. Anschließend erfolgt das Tempern im Rohrofen. Dabei diffundiert das Kupfer durch das Substrat und die BOX (buried oxide) in den SOI/sSOI-Film und präzipitiert als Kupfersilizid (Cu_3Si) beim Quenschen auf Raumtemperatur hauptsächlich an Kristalldefekten, in denen die Kristallgitterverspannung größer als im perfekten Kristallgitter ist. Diese Silizide dehnen das Volumen am Kristallgitter an der Stelle des Defektes aus, was zur Vergrößerung der Defekte führt. Ein bedenklicher Nachteil dieser Methode ist die Tendenz der Artefaktbildung, wenn die eingesetzte Kupferkonzentration zu hoch ist. Dabei präzipitiert das Kupfer auf der Siliziumoberfläche. Daraus resultiert eine höhere Defektdichte an Ätzfiguren, wodurch echte Ätzfiguren, die ihren Ursprung in Kristalldefekten haben, nicht von den durch Artefakte erhaltenen Ätzfiguren unterschieden werden können.

Ziel dieser Dissertation ist es zu zeigen, dass die beiden Prozesse Dekoration und Ätzung miteinander für einen erfolgreichen Nachweis aller Kristalldefekte in SOI und sSOI kombiniert werden können. Ein ideales Ergebnis wäre die Entwicklung einer Dekorationsmethode, in der die Dekoration aller vorliegenden Kristalldefekte bei einer Kupferkonzentration erfolgt, welche keine Artefakte induziert.

Die Schichtdicken der verwendeten SOI und sSOI Wafer waren 60-1 400 nm (SOI) und 14-84 nm (sSOI). Die nachgewiesenen Defekte waren Crystal Originated Partices (COPs) (Leerstellenagglomerate), „Red Spots“ und Oxidation induced Stacking Faults (OiSF) in SOI und prozessinduzierte Stacking Faults (SF) und Threading Dislocations (TD) in sSOI. Zwei Arten an Defekte konnten in thick SOI nachgewiesen werden: Defekte mit und Defekte ohne einen Hof. Defekte mit einem Hof könnten ihren Ursprung in den oberen Bereichen den SOI-Films haben. Hierbei entsteht der Hof dadurch, dass die BOX während des HF Dips weggeätzt wird. Defekte ohne einen Hof könnten in den tieferen Bereichen des SOI-Film vorliegen. Hier wird während des HF Dips die BOX unter dem Defekt nicht weggeätzt, wodurch es zu keiner Bildung eines Hofes kommt.

Die dilute Secco (0.04 M Cr (VI)) wurde für die beiden Materialien SOI und sSOI als die Standardätzlösung verwendet. Darüber hinaus fanden weitere Ätzlösungen wie OPE (SOI, sSOI), CP4 (610 nm SOI), CA (Standard SOI) und Jeita (1 400 nm SOI) als chromfreie Alternativen ihren Einsatz. Bei Jeita A und B handelt es sich um zwei alternative Ätzlösungen, welche speziell für den Nachweis von Kristalldefekten in thick 1 400 nm SOI bedingt durch ihre höhere Ätzrate verwendet wurden. Jeita A setzt sich aus HNO_3, HF und HAc zusammen, Jeita B beinhaltet zusätzlich KI. Alle Resultate aus den unterschiedlichen Experimenten mit der jeweiligen geeigneten chromfreien Ätzlösung wurden mit den entsprechenden Ergebnissen nach der Secco Ätzung verglichen. Die Hauptkriterien für die Wahl der geeigneten Ätzlösung waren die Schichtdicke des SOI/sSOI-Films und die Ergebnisse aus bereits von anderen durchgeführten Untersuchungen in diesem Bereich an nicht dekorierten Proben. Die Ätzdauer wurde variabel an die Schichtdicke des SOI/sSOI-Films und an die Ätzrate der eingesetzten Ätzlösung angepasst.

Es wurde zwischen zwei Arten an Referenz-Proben unterschieden: nicht dekorierte und nicht getemperte Proben (Ref 1) und nicht dekorierte, aber getemperte Proben (Ref 2). Die Kupfer dekorierten Proben wurden mit beiden Referenzarten (wenn vorhanden) in Bezug auf die ermittelte Defektdichte (DD) und die Defektcharakterisierung verglichen. Für die Defektcharakterisierung fanden die Lichtmikroskopie, die Rasterkraftmikroskopie (AFM) und die Rasterelektronenmikroskopie (REM) ihren Einsatz.

Zur Vermeidung der Artefaktbildung während des Temperns im Rohrofen wurde eine andere Methode zur Dekoration der Kristalldefekte in SOI und sSOI untersucht. Dabei erfolgte die Abscheidung von Kupfer ausgehend von einer verdünnten $Cu(NO_3)_2$-haltigen HF-Lösung auf elektrochemischen Weg. Im Anschluss wurde mit einer dilute Secco geätzt. Als Ergebnis konnte die Abscheidung und das Wachstum von Kupferpartikel auf der Probenoberfläche beobachtet werden. Daraus folgte nach dem Ätzen eine deutlich erhöhte Anzahl an Ätzfiguren verglichen zu der DD nach der Dekoration mittels Tempern im Rohrofen. Das

Fazit aus diesen Experimenten war, dass die elektrochemische Kupferabscheidung ungeeignet für den Nachweis der COPs in SOI ist. Weitere Experimente zum Nachweis von Stacking Faults und Threading Dislocations in sSOI führten jedoch zu erfolgreichen Ergebnissen beim Einsatz einer 0.1 ppm Kupfer haltigen Lösung.

Die Dekoration mittels Tempern im Rohrofen wurde anschließend die Standard Dekorationsmethode für verschiedene SOI Wafer mit unterschiedlichen Schichtdicken. Hierfür wurden die experimentellen Parameter für jeden Probentyp entwickelt und optimiert. Für die Sichtbarmachung von Kristalldefekten in Standard SOI mit Schichtdicken im Bereich von 60-149 nm wurden sowohl verschiedene chromfreie Ätzlösungen, als auch die dilute Secco verwendet.

Die OPE D wurde unter anderem zum Ätzen von mit Kupfer dekoriere Standard SOI Proben eingeätzt. Die gebildeten Ätzfiguren wiesen einen deutlich größeren Radius im Vergleich zu den Ätzfiguren nach einer Ätzung mit der dilute Secco auf. Die Ätzrate der OPE D ist im Vergleich zur dilute Secco niedriger. Die längere Ätzzeit führt zur Ausbildung größerer Ätzfiguren von Defekten, welche sich in der Nähe der Probenoberfläche befinden und zur Ausbildung kleinerer Ätzfiguren von Defekten, welche sich im unteren Bereich des SOI-Films vorliegen. Es wurden höhere Defektdichten nach dem Ätzen mit OPE D ermittelt.

Die Defektdichten von prozessinduzierten OiSF in 90 nm SOI Wafer wurden ebenfalls bestimmt mit dem Ziel diesen Defekttyp während der Waferproduktion zu vermeiden. Hierfür wurde die Chloranil (2,3,5,6-Tetrachloro-1,4-Benzoquinon) Ätzlösung als chromfreie Variante zur dilute Secco für die Sichtbarmachung der OiSF eingesetzt und ihre Effizienz untersucht. Diese Experimente bewiesen nach dem Einsatz beider Ätzlösungen, dass ab einer Kupferkonzentration von und über 0.01 ppm die Defekte dekoriert wurden. Die Dekoration mit diesen Kupferkonzentration führten zu einer verbesserten Sichtbarmachung der OiSF nach der Ätzung mit der weniger sensiblen CA Lösung. Dennoch konnten die Ergebnisse nach der CA-Ätzung nicht an die Effektivität der dilute Secco erreichen, welche ein höheres Oxidatiospotential aufweist.

Weitere Kupferdekorationsexperimente wurden mit verschiedenen thick SOI Wafer durchgeführt (610 nm SOI mit einer 300 nm BOX und 1 400 nm SOI mit einer 1 000 nm BOX). Die Parameter für die Dekoration wurden entsprechend der dickeren Schichten entwickelt und optimiert. Beide Probentypen weisen eine recht dicke BOX-Schicht auf, welche als Diffusionsbarriere für das Kupfer angesehen werden kann. Bei einer Temperungstemperatur von 900 °C für die 300 nm BOX und 950 °C für die 1 000 nm BOX konnte genügend Kupfer durch die BOX in die SOI-Schicht diffundieren und die Dekoration der Defekte erfolgte.

Die 1 400 nm SOI Proben wurden zum einen mit der dilute Secco und zum anderen mit den Jeita A und B Lösungen geätzt. Das höhere Oxidationspotential und die höhere Selektivität der dilute Secco führten zu einer besseren Sichtbarmachung der Defekte mit einem Halo, während die Jeita A und B Lösungen eine höhere DD an kleinen Pits erzeugten. Die beste Kupferkonzentration für die Sichtbarmachung der Defekte in 1 400 nm thick SOI scheint im Bereich von 0.01 und 0.1 ppm nach dem Ätze mit der dilute Secco zu sein. Jedoch konnte nach dem Ätzen mit Jeita A oder B kein klarer Trend zwischen der eingesetzten Kupferkonzentration und der ermittelten DD für die Defekte mit und ohne Halo erkannt werden. Eine mögliche Erklärung könnte ihr niedriges Oxidationspotential und ihre niedrige Selektivität sein.

SOI Wafer mit einer Schichtdicke von 610 nm und einer 300 nm BOX wurden nach der Dekoration mit Kupfer zum einen mit CP4 + KIO_3 (CP4 A) und CP4 + KIO_3 + KI (CP4 B) und zum anderen mit der dilute Secco geätzt. Nach dem Ätzen mit der dilute Secco wurde bei einer Kupferkonzentration von [Cu]≥ 0.1 ppm ein An stieg der DD beobachtet. Die höchste DD konnte bei den mit Secco geätzten Proben, im Vergleich zu den DD nach der Ätzung mit CP4 A bzw. CP4 B, beobachtet werden. Es wurde kein klarer Trend zwischen Kupferdekoration und DD festgestellt (CP4 B). Weder die CP4 A noch die CP4 B führten zu DD, die den mittels dilute Secco ermittelten entsprachen.

Die optimale Kupferkonzentration für alle getesteten Ätzlösungen und alle untersuchten SOI und sSOI Schichtdicken lag immer im Bereich von 0.01-0.1 ppm für die Dekoration der unterschiedlichen Kristalldefekte. In diesem Konzentrationsbereich konnte die Dekoration der Defekte erzielt und gleichzeitig eine mögliche Artefaktbildung weitgehends vermieden werden. In allen Fällen diffundierte das Kupfer durch die BOX, welche eine Schichtdicke im Bereich von 145 nm bis 1 000 nm aufwies. Entsprechend der BOX Schichtdicke wurde die Temperungstemperatur zwischen 800-950 °C variiert.

Chromfreie OPE Lösungen wurden als Alternative zu der Secco Ätzlösung zur Sichtbarmachung von Kristalldefekten in sSOI untersucht. Verschiedene OPE Lösungen wurden mit unterschiedlichen Kupferkonzentrationen getestet, um nicht nur die TD, sondern auch die SF sichtbar zu machen. Die besten Resultate hierfür wurden mit der OPE B Lösung erhalten. Die experimentellen Parameter für die Kupferdekoration mit anschließender OPE B Ätzung wurden entwickelt und optimiert.

Weitere Untersuchungen für die Dekoration und Ätzung von Kristalldefekten wurden an 200 nm SIMOX Proben mit einer BOX Schichtdicke von 95 nm, welche stark verkratzt waren, durchgeführt. Bei den Kristalldefekten handelte es sich um COPs und zu einem großen Anteil um Prozess-induzierte Sauerstoffpräzipitate, die sich hauptsächlich in der Nähe von

der Silizium Film/BOX Zwischenschicht befanden. Aus diesem Grund wurde der Silizium-Film bis in die Nähe der BOX im Vergleich zum SOI runter geätzt. Die Kupferdekoration führte zu einer verstärkten Sichtbarmachung der Defekte und somit zu einer höheren DD. Die chromfreie OPE B Lösung führte nach dem Ätzen zu vergleichbaren DD wie die dilute Secco. Deshalb kann die OPE B als Alternative für die dilute Secco zum Nachweis der Kristalldefekte in SIMOX eingesetzt werden.

In der Vergangenheit wurde die Lithiumdekoration erfolgreich als Alternative für die Dekoration der Kristalldefekte in Silizium Wafer eingesetzt [93], weil kaum bzw. keine Artefaktbildung beobachtet werden konnte. Da Lithium eine hohe Sauerstoffaffinität aufweist, ist die Dekoration und somit die Diffusion von Lithium in SOI und sSOI bedingt durch die BOX problematisch. Untersuchungen für die Dekoration mittels Lithiumnitrat von Standard SOI und neuem extra thin SOI (20 nm) mit einer ultra-thin BOX (10 nm) (ETSOI/UTBOXSOI) wurden durchgeführt. Diese Dekorationsexperimente führten leider nicht zu den erhofften Ergebnissen. Weitere Experimente hätten den Rahmen dieser Dissertation gesprengt, deshalb wurden Untersuchungen für die Verteilung des Lithiums nach der Diffusion im SOI Wafer bevorzugt. Während das Lithium leicht durch die ultra-thin BOX diffundierte, stellte sich die BOX (145 nm) im Standard SOI als Diffusionsbarriere heraus. Die Ergebnisse zeigten weiterhin einen Gasphasentransport des Lithiums im Rohrofen während des Temperns, wodurch das Lithium von der Vorderseite, dem SOI-Film, die Kristalldefekte dekorierte.

Der Einfluss der Metalldekoration auf den Ätzprozess der Kristalldefekte in Standard SOI wurde in Bezug auf die Parameter Abtragsrate, Selektivität und Aktivierungsenergie für den Ätzprozess untersucht.

Die Selektivität der dilute Secco wurde experimentell in Kupfer und Lithium dekorierten und nicht dekorierten Czochralski (CZ) Silizium Bulk Proben bestimmt. Wie erwartet konnte bestätigt werden, dass die Selektivität für die Versetzungen in der Referenzprobe am niedrigsten war. Nach der Dekoration mit 0.0001-1 ppm an Kupfer oder Lithium stieg die Selektivität stark an. Bei der Kupferkonzentration 10 ppm war der Grad der Kupferpräzipitation sehr hoch.

Die Abtragsrate der dekorierten SOI Proben unterschied sich nicht von denen der nicht dekorierten Proben. Mit Hilfe eines Ellipsometers wurde die Restschichtdicke nach dem Ätzen der SOI-Schicht ermittelt. Dabei wurde die Schichtdicke an verschiedenen Stellen der Probenoberfläche gemessen. Da die DD der Proben sehr gering waren, konnte die Schichtdicke der Defekte auf diesem Wege nicht ermittelt werden. Somit waren die

bestimmten Aktivierungsenergien, wie bereits erwartet, unabhängig von den Schichtdicken des SOI.

Die erfolgreiche Entwicklung der Dekorations- und Ätzmethoden führt zu einer deutlichen Verbesserung der Sichtbarmachung der Kristalldefekte in SOI und sSOI Halbleitermaterialien mit verschiedenen Schichtdicken.

6 Appendix

6.1 Etchants used

Etching solution	Composition
“Chloranil (CA)”-solution	0.5 g Chloranil in 120 mL dioxane 30 mL HF (49%)
CP4 + KIO_3	72 mL acetic acid 70 mL HNO_3, 2 mL HF (49%) 0.232 g KIO_3
CP4 + KIO_3 + KI	72 mL acetic acid 70 mL HNO_3, 2 mL HF (49%) 0.0213 g KIO_3 0.041 g KI

Dilute Secco (0.04 M Cr (VI))	0.6 g $K_2Cr_2O_7$ in 100 mL H_20
	50 mL HF (49%)
Dilute Secco (0.02 M Cr (VI))	0.3 g $K_2Cr_2O_7$ in 100 mL H_20
	50 mL HF (49%)
Jeita A	90 mL HNO_3
	36 mL acetic acid
	36 mL H_20
	6 mL HF (49%)
Jeita B	90 mL HNO_3
	36 mL acetic acid
	36 mL H_20
	6 mL HF (49%)
	402 µL of a 0.1 KI solution (1.66 g KI in 100 mL H_2O)
OPE A	43 mL H_2O_2 (30%)
	14.5 mL HF (49%)
	143 mL acetic acid

OPE B	43 mL H_2O_2 (30%)
	43 mL HF (49%)
	114 mL acetic acid
OPE D	50 mL H_2O_2 (50%)
	50 mL HF (49%)
	100 mL propanoic acid (100%)
OPE F	75 mL H_2O_2 (50%)
	5 mL HF (49%)
	120 mL acetic acid

6.2 Cleaning procedure for the quartz tubes and vessels

A further source for artefact formation is the residual copper in the quartz tubes and reaction vessels used. Therefore, all the vessels and quartz tubes were cleaned periodically to avoid this copper cross contamination. The cleaning procedure was performed as follows:

- The vessels and quartz tubes were put in a weak concentrated RBS solution for 10 min in a ultra sonic bath
- Subsequently the tubes and vessels were cleaned in water for 10 min in a ultra sonic bath
- In the next step the vessels and quartz tubes were put in a weak concentrated HNO_3 solution for 10 min in a ultra sonic bath
- Then the tubes and vessels were cleaned in water for 10 min in a ultra sonic bath

6.3 Instruments used

- **Light optical microscope**
  Reichert Univar

  Digital camera: Leica DFC 280

  Software: Leica IM 50 Image Manager

- **Scanning electron microscope (SEM)**
  Atomica/Amray 1920 Eco Environment controlled SEM

- **Atomic force microscope (AFM)**
  Digital Instruments Nano Scope III a

  AFM-tips: Olympus Standard Silicon probe OMCL-AC160TS-C2

- **Indentor**
  Mikro-Härteprüfer VMHT-MOT Leica UHL

- **Profilometer**
  Tencor Instruments alpha-step 200

- **Ellipsometer**
  Plasmos SD 2000

- **Thermostat**
  VWR Kältethermostat 1160 S

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EDUCATION

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Oct. 2000 – June 2007	Studied chemistry and pharmacology (elutive) at the above-named University
June 2007	Obtained a “Diplom” (Master´s degree) with the thesis “Decoration and etching of crystal defects in semiconductor materials”
Aug. 1991 – June 2000	Attended and successfully completed secondary school at the Max-Planck Gymnasium in Rüsselsheim
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Eidesstattliche Erklärung

Hiermit erkläre ich an Eidesstatt, dass die vorliegende Arbeit von mir eigenständig und nur unter Verwendung der genannten Hilfsmittel und Literatur angefertigt wurde.

Statutory Declaration

I hereby declare that this submission is my own work and has been prepared with the resources and literature duly referred to in the text.

Frankfurt am Main, März 2013.

Hanan Idrisi